

OPERATION / MAINTENANCE MANUAL

TRANSCEIVER TEST SET

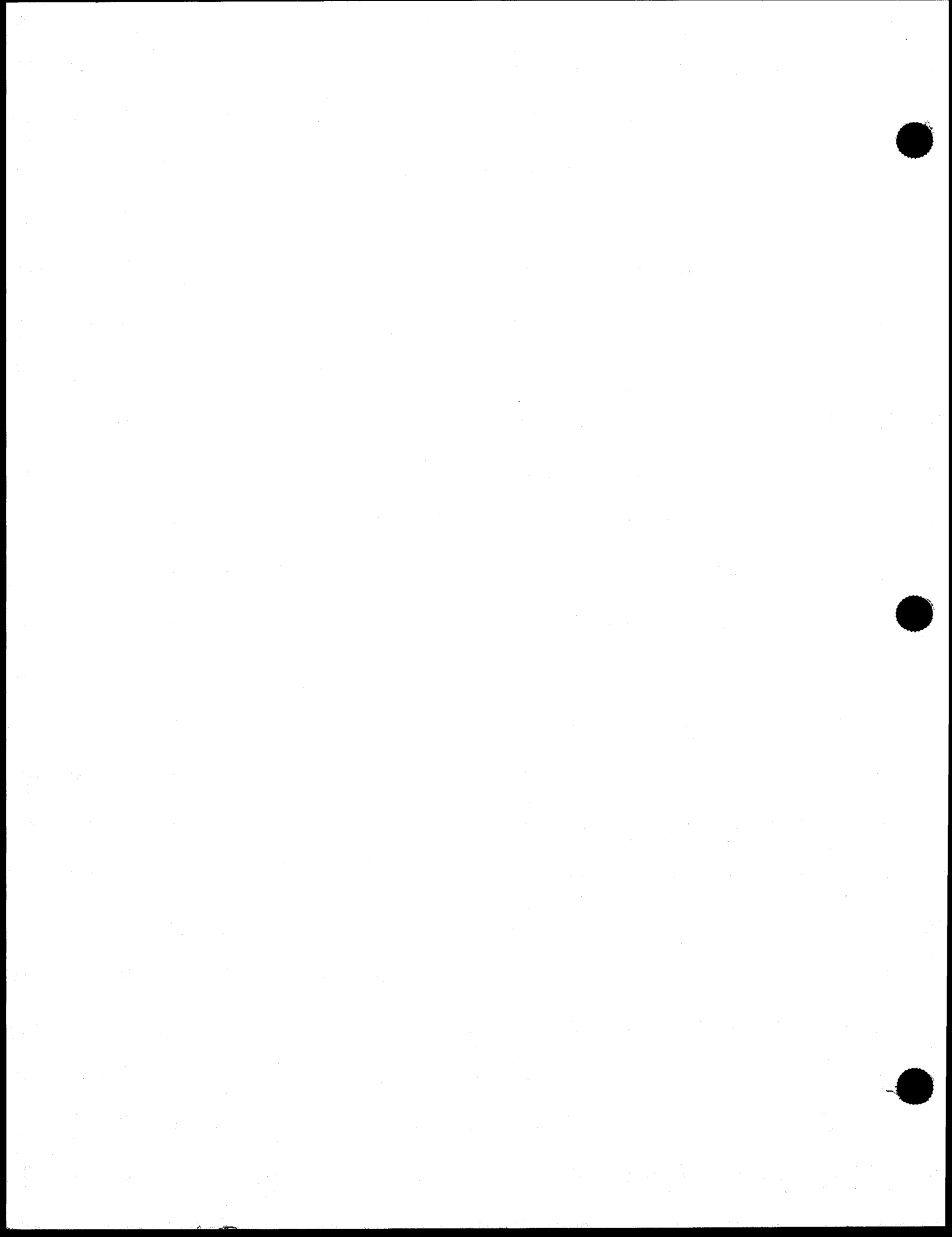
COMM-760

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IFR AMERICAS, INC.**

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COMM 760

NOTICE

To insure correct cable (P/N 2-17-0059) connection to your NAV 750, one pin connection is disconnected.

To match Comm 760 S/N 150 & up to NAV 750/A S/N thru 421 & 468 & 469 insert loose wire terminal into connector position 1.

To match Comm 760 S/N 150 & up to NAV 750/A S/N 422 thru 467 & 470 & up and NAV 750B 2001 & on, insert loose wire terminal into connector position 6.

An extra cable, IFR P/N 2-17-0059, may be ordered separately.

NOTE

External 50 ohm load on NAV 750 External Mod jack must be removed when Comm 760 is used to modulate the NAV 750.



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SECTION I

Description

- 1-1. The COMM-760 Test Set is designed to facilitate the testing of each of the 720 or more channels on modern, remotely programmable or manually operated communications transceivers.
- 1-2. The Test Set measures the receiver audio output level or Signal + Noise-to-Noise ratio, S+N/N, (using an external signal generator) and the transmitter frequency and power. When teamed with the NAV-750 signal generator's automatic channelling capability, these parameters are measured in rapid go/no-go checks of each channel until any parameter falls outside selectable limits.
- 1-3. Measurement of the transmitter's modulation sensitivity is possible with the Test Set's audio oscillator, voltmeter, and percent-of-modulation circuitry. The oscillator can also be used to check the receiver's frequency response and carrier override squelch threshold.
- 1-4. A microphone input is provided, as well as an attenuated sample of the transmitter output, both direct and detected, for oscilloscope use.
- 1-5. For transmitter channel frequency error measurements, the actual transmitter frequency and the difference between the NAV-750-commanded frequency and the transmitter frequency is displayed.
- 1-6. The receiver's S+N/N is measured with automatic level control, active filter, and IC analog divider circuitry to insure that correct results are obtained over a wide range of receiver audio output levels.
- 1-7. A back panel printer output allows listing of the channel frequency and type of fault for each channel or only those channels on which a fault occurs. The printer output interfaces with a number of 8 or 10 column output digital printers such as the HP-5055A or the Fluke 2010A.

SPECIFICATIONS

Receiver Measurements:

Audio Output Signal	0-10V into 500 (± 50) ohm, $\pm 3\%$ fs, 50 to 5000Hz.
Signal + Noise/Noise Ratio	0-14dB, ± 1 dB; modulation frequency of 1020 ± 5 Hz; receiver audio levels of 0.1 to 8V rms.

Transmitter Measurements:

Frequency	117-156 MHz (Ovened time base; crystal aging: 3 PPM first year, 1 PPM afterwards; ± 1 count)
Channel Frequency Error Display	0-19.9 kHz (Accuracy is based on above stability, e.g., a 1 PPM drift represents a ± 0.1 kHz error here; ± 1 count)
Error Limit Threshold	0-9.9 kHz
Power	0-100W, $\pm 5\%$ fs (Bird Corp "Thruline" Wattmeter)
ANT Input VSWR	1.25:1
Percent Modulation	0-95% $\pm 3\%$ fs, 300Hz to 3 kHz

Detector:

Residual Hum & Noise	2mV rms
T.H.D.	3% max @ 90% AM
Output Level	AGC amplifier output: -2.2V dc (nominal) for carriers 5W to 50W; 100% AM equals 0.78V rms (nominal)

Modulation Tone Generator:

Fixed: 1020 ± 10 Hz. Variable 150Hz to 13 kHz; 0-1.8V rms into 100 ohm, 3% THD Max (0.5% typical at 1020Hz)

Dimensions:

5.0" (12.7cm) high, 16.8"
(42.7cm) wide, 18.4"
(46.7cm) deep.

Weight:

15 pounds (6.8kg)

A.C. Power:

105 to 120 VAC or 220 to
250 VAC, 50 to 400Hz, 75W.



LIMITED WARRANTY AND SERVICE INSTRUCTION

- A. Limited Warranty.
- B. IFR, Inc., warrants that each new instrument manufactured by it is free from defects in material or workmanship under normal use and service for a period of two years from the shipping date. Each instrument is functionally tested immediately prior to shipment. If, upon examination by IFR, the instrument is determined to be defective in workmanship or material, IFR will, subject to the conditions set forth below, either repair the defective part or replace it with a new part on a pro rata basis. IFR shall not be liable for any delay or failure to furnish a replacement part resulting directly or indirectly from any governmental restriction, priority or allocation or any other governmental regulatory order or action, nor shall IFR be liable for damages by reason of the failure of the instrument to perform properly or for any consequential damages. The warranty does not apply to any instrument that has been subject to negligence, accident, shipping damage, misuse or improper installation or operation, or that in any way has been tampered with, altered or repaired by any person other than an authorized IFR service organization or any employee thereof, or to any instrument whose serial number has been altered, defaced or removed, or to any instrument purchased within, and thereafter removed beyond, the continental limits of the United States. Annual recalibration is not included in warranty.
- C. All sales are fob IFR factory, Wichita. IFR will assume responsibility for freight charges on all legitimate warranty claims within thirty (30) days from the original shipping date. All legitimate warranty claims within thirty (30) to ninety (90) days should be shipped to IFR freight collect and will be returned freight collect. All freight on warranty claims after ninety (90) days will be paid by the customer.
- D. This warranty shall, at IFR's option, become void if the equipment ownership is changed, unless the prior owner or the proposed owner obtains approval of continuation of the warranty prior to the change of ownership.
- E. This warranty is in lieu of all other warranties, expressed or implied, and no one is authorized to assume any liability on behalf of IFR or impose any obligation upon it in connection with the sale of any instrument, other than as stated above.
- F. Changes in Specifications.
- G. The right is reserved to change the published specifications of the equipment at any time and to furnish merchandise in

accordance with current specifications without incurring any liability to modify equipment previously sold, or to supply new equipment in accordance with earlier specifications except the classification of special apparatus.

H. Service.

- I. When requesting service, the originator shall give IFR information concerning the nature of the failure and the manner in which the equipment was used when the failure occurred. Type, model, and serial number should also be provided.
- J. Do not return any products to the factory without first receiving authorization from the factory Customer Service Department.

CONTACT:

IFR SYSTEMS, INC.
10200 West York Street
Wichita, Kansas 67215 USA

ATTN: Customer Service Department

PHONE: (800) 835-2350 (Customer Service Only)

TWX: 910-741-6952

- K. Unless otherwise specifically requested, packaging for a return shipment shall be in the original container and packaging material. If the original container and material are not available, information as to suitable packaging techniques will be provided by the IFR Shipping Department.
- L. Returned material claimed defective, but found to meet all previously applicable specifications, will be subject to a minimum evaluation charge consisting of the labor charges involved in the status determination of the material.
- M. Returned material not accompanied by statement of claimed defects may be returned at the originator's expense.
- N. Any departure from the above instructions without specific factory authorization can be considered a breach of warranty, and all expenses incurred as a result will be billed to the originator.



SECTION II

Inspection

2-1. Inspection After Shipping.

- 2-2. This instrument was carefully inspected both mechanically and electrically before shipment. It should be physically free of marks and scratches and in perfect electrical order upon receipt. To confirm this, the instrument should be inspected for physical damage occurring in transit. Also, check all supplied accessories, and test the electrical performance of the instrument using the procedure outlined in Section V of this manual. If there is any damage or deficiency, file a claim with the carrier, and refer to the Warranty portion in Section I of this manual. If it should become necessary to ship the instrument, refer to paragraph K page 1-W.1 for shipping instructions.

2-3. Grounding Requirements.

- 2-4. To protect operating personnel, the National Electrical Manufacturer's Association (NEMA) recommends that the instrument panel and cabinet be grounded. All IFR, Inc. instruments are equipped with a three-conductor power cord which, when plugged into an appropriate receptacle, ground the instrument. The offset pin on the power cord three-prong connector is the ground connection.
- 2-5. To preserve the protection feature when operating the instrument from a two-contact outlet, use a three-prong to two-prong adapter and connect the grounding pigtail on the adapter to ground.

2-6. Rack/Bench Installation.

This instrument is initially shipped as a bench-type instrument, (unless ordered specifically as a rack type) with plastic feet in place. Conversion to a rack-mounted instrument can be accomplished by using the Rack Mounting Kit available from the factory upon request.

2-7. Repackaging for Shipment.

- 2-8. The following is a general guide for repackaging for shipment. If there are any questions, contact the IFR, Inc. Shipping Department. (See page 1-W.1 paragraph K)

————— NOTE —————

If the instrument is to be shipped to IFR, Inc. for service or repair, attach a tag to the instrument identifying the owner and indicating the service or repair to be accomplished; include the model number and full serial number of the instrument. In any correspondence, identify the instrument by prefix, model and serial number.

Place instrument in original container if available. If original container is not available, contact IFR, Inc. for shipping instructions.

Do not return the instrument or its component parts to IFR, Inc. for repair without first receiving authorization from IFR, Inc. Refer to paragraph H page 1-W.1 for complete instructions.

Inspection/Check

2-9. Introduction.

2-10. This section presents instructions to determine, by inspection, the general condition of the COMM-760 and locate possible faults through either normal operation or performance tests.

2-11. IFR, Inc. has determined by experience that deliberate moving, however slight, of the discrete components on the various PC boards or other assemblies, will often cause circuit problems which were not originally causes of problems. This can quickly change simple problems into complex ones. Therefore the factory recommends only a close visual inspection without touching the components.

2-12. Cleaning.

2-13. Remove all dust, foreign matter etc., from inside test set prior to inspection, repair, or calibration. This test equipment should be cleaned on a regular basis such as bi-annual or annual proof-of-performance checks.

2-14. It is recommended that dust removal be done with a hand controlled dry air jet of not too high pressure (25-50 psi). The fan blades, rotor and frame should be wiped with a lint-free cloth moistened with rubbing alcohol. The rear panel should be cleaned with a dry cloth only. The front panel may be cleaned whenever necessary with a lint-free cloth moistened with rubbing alcohol.

2-15. Care must be taken to avoid breaking wires or shorting component leads together during cleaning.

2-16. Inspection/Check.

2-17. Procedures.

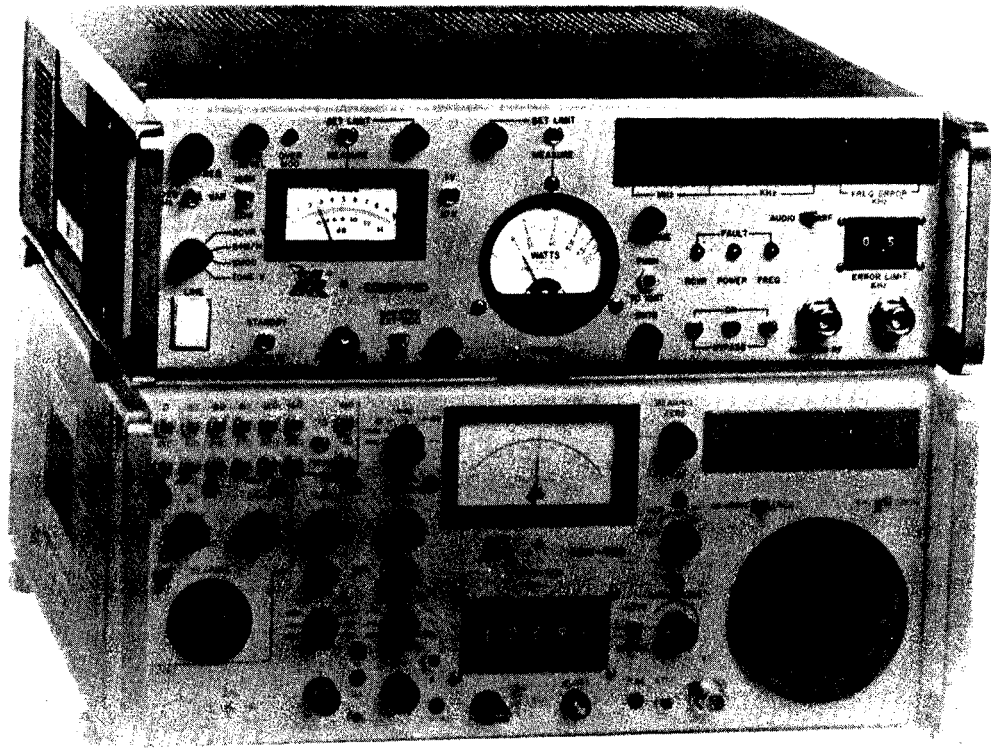
A. Chassis. Includes anything mechanical or made from metal. Inspect for tightness of sub-assemblies, damaged connectors, corrosion or damage to the metal surfaces etc. Surface corrosion may indicate damage inside the affected part.

- B. Capacitors. Inspect for loose mounting, body damage, case damage, leakage or corrosion around leads.
- C. Jacks. Inspect all coax jacks for loose or broken parts, cracked insulation, bad contacts, etc. Do not disassemble connectors within the test set.
- D. Potentiometers. Any potentiometer that feels rough when rotated or produces circuit or voltage irregularities should be checked with an ohmmeter for proper operation.
- E. Resistors. Inspect all types of resistors for cracked, broken, charred or blistered bodies and loose or corroded soldering connections.
- F. Printed Circuit Boards. Check connectors for corrosion or damage and the mating plugs for similiar damage. Inspect all mounted components for damage including crystals and IC's. The board should be free of all foreign material.
- G. Semiconductors. Inspect all diodes, rectifiers and transistors for cracked, broken, charred or discolored bodies. Check ends of components for seals around leads.
- H. Switches. Examine all toggle switches for loose levers and terminals, loose body to frame condition. The line switch contacts should not be bent nor the switch action too loose. The thumbwheel switches should have definite detents and not feel loose.
- I. Transformer. Inspect the transformer for signs of excessive heating, broken or charred insulation, loose mounting hardware and other abnormal conditions.
- J. Wiring. Inspect all wiring of chassis for broken or loose ends, loose connections and proper dress relative to other chassis parts. All laced wiring should be tight with ends securely tied.

SECTION III

Operation

- 3-1. Introduction.
- 3-2. This section contains instructions and information necessary for operation of the IFR Model COMM-760 Transceiver Test Set.
- 3-3. Included in this section are identification of front and rear panel controls, indicators, and connectors, as well as operation with equipment being tested and information useful in applications for transceiver testing. The controls are identified in Fig 3-1. Step by step procedures for testing a transceiver are contained in this section beginning with Paragraph 3-14, Page 3-16.





SECTION III

Test Set Operation

3-4. Controls, Connectors and Indicators.

- 3-5. This section contains a description of the function of each control, connector, or indicator on the test set. The controls are identified in Fig 3-1. Step-by-step procedures for testing a transceiver are contained in this section.
- 3-6. Figure 3-3 is an equipment interconnection diagram for the test set, NAV-750 Signal Generator, Unit Under Test, Printer, and Oscilloscope.
- 3-7. Table 3-1 is a pinout table for the interconnection to the Unit Under Test (U.U.T.). Table 3-2 is a pinout table for the interconnection to the printer. Table 3-3 is a typical format for the printer output.
- 3-8. The following paragraphs describe the printer control signals at J-3. (Refer to Table 3-2 for J-3 pinout and Fig 4-3 for timing diagrams). All controls signals are TTL levels.
- 3-9. FREQ, POWER, RCVR FAULT B (J3-1,2,3). If a fault has occurred these lines will be low during the printer's cycle.

NOTE

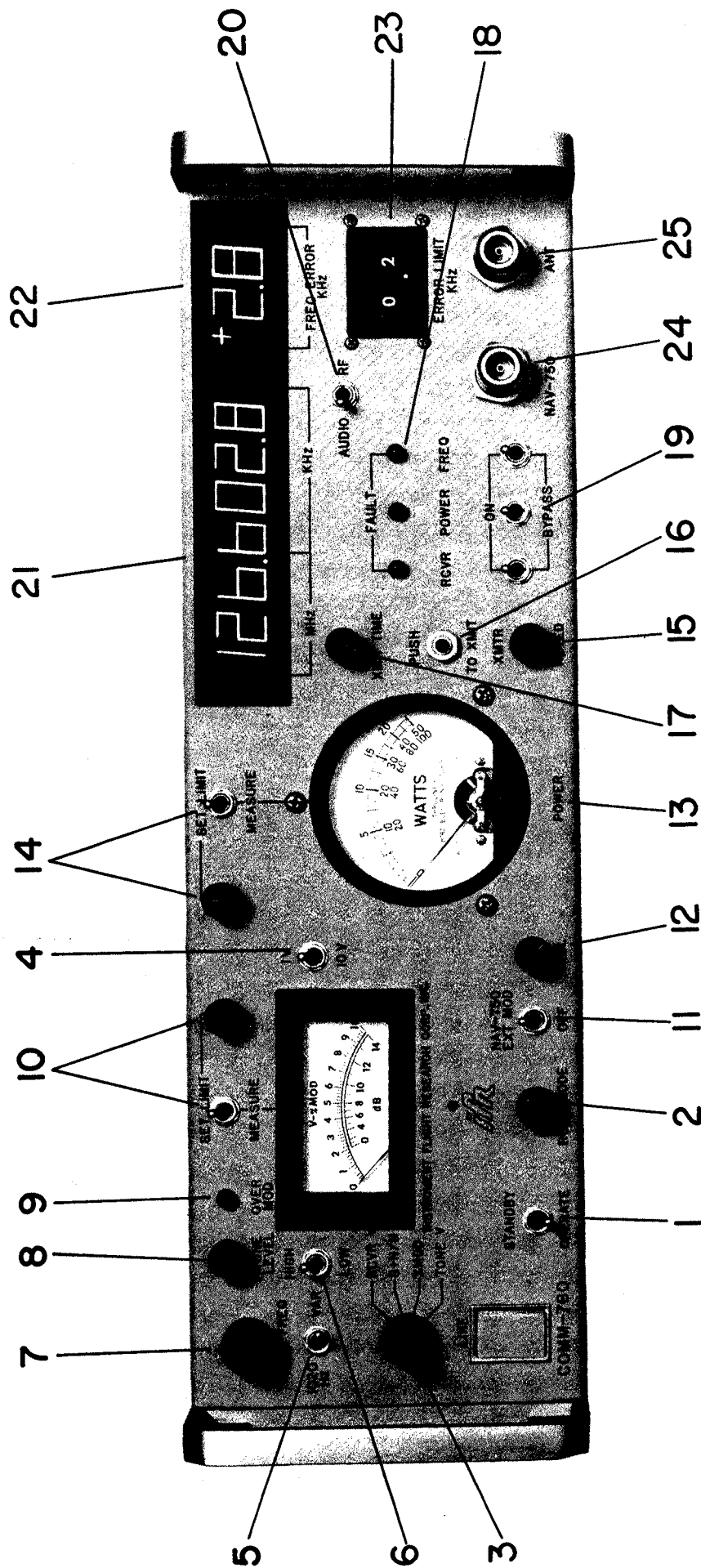
In Fig 4-3 PWR FLT B and FREQ FLT B resets HI while RCVR FLT B resets LOW between print commands. See Fig 4-3.

- 3-10. PRINTER INHIBIT IN (J3-39), PRINTER INHIBIT IN (J3-38). These lines connect to the printer's Inhibit or Busy output which remains active from the reception of a print command until the end of the printer's cycle. Both high and low active inputs are available. If the printer has no Inhibit or Busy output, see below.
- 3-11. PRINTER INHIBIT OUT. (J3-40) For printers with no Inhibit or Busy output, this line simulates a printer Inhibit signal and should be jumpered to PRINTER INHIBIT IN (J3-38). This line is active (LOW) for 0.36 seconds before system reset occurs and the NAV-750 advances to the next channel. If the printer used takes longer than 0.36 seconds to complete its cycle, increase C218 on the Main Circuit Board according to the relation $t = 0.011 \times C218$ where C218 is in microfarads and t is the time necessary to complete a print cycle (C218 is electrolytic, 20V).

- 3-12. PRINT COMMAND (J3-41), ~~PRINT COMMAND~~ (J3-42). Control lines to start the printer cycle. Pulse width is 25ms.
- 3-13. Channel Frequency BCD Output (J3 various). These high active lines control the channel frequency printout for the 10, 1, 0.1, 0.01, and 0.001 MHz decades. The printer column corresponding to the 100 MHz decade should be hardwired to logic 1 to print a 1. The columns corresponding to 0.01 and 0.001 MHz should be wired as follows:

<u>DECADE</u>	<u>BCD BIT</u>	<u>COMM-760 BCD OUTPUT</u>
0.01 MHz	8. . . .	N.C. or Logic 0
	4. . . .	0.05 MHz
	2. . . .	0.025 MHz
	1. . . .	0.05 MHz
0.001 MHz	8. . . .	N.C. or Logic 0
	4. . . .	0.025 MHz
	2. . . .	N.C. or Logic 0
	1. . . .	0.025 MHz

- 3-14. Frequency Error BCD Output (J3-18 to J3-25). These high active lines control the frequency error printout for the 1.0 and 0.1 kHz decades.
- 3-15. Frequency Error Sign Control (J3-43,44). These high active lines control the printout of the sign of the frequency error printout. J3-43 will be logic 1 when the frequency error is negative or there is no frequency being counted.



FRONT PANEL CONTROLS, CONNECTORS
AND INDICATORS

FIG. 3-1

3-16. Functional Description of Front Panel Controls, Connectors, and Indicators. (See Fig 3-1)

1. STANDBY/OPERATE. In STANDBY, Unit Under Test (U.U.T.) and test set remain in the Receive mode unless the PUSH TO XMIT button is depressed. This position will also stop the repetitive channel advance command to the NAV-750 and will stop the printer. However, manual channel advance and printer operation are possible by depressing PUSH TO XMIT. In OPERATE, the test set will start the tests on the U.U.T. starting from the channel selected on the NAV-750 FREQUENCY switch. See paragraph 16 and Note 1 below.
2. RCVR Mode. When lighted, the U.U.T. is in its receive mode and Receiver audio output level (RCVR V) or signal-plus-noise-to-noise ratio ($S + N/N$) measurements can be made either manually (STANDBY mode) or automatically (OPERATE mode).
3. Meter Function Switch. In RCVR V (Receiver output Volts) position, the meter measures the receiver audio output level across a 500 ohm load at either 1 or 10 volts full scale as selected by the switch to the right of the meter. The fault decision level for this measurement is adjusted by the SET LIMIT (volts) control and switch above the left hand meter.

In $S + N/N$, the Signal-plus-noise-to-noise ratio at the U.U.T.'s receiver audio output is measured in dB using RF from the NAV-750. The normal modulation is 30% AM, 1020Hz. (See note 2) The fault decision level is fixed at 6dB.

————— NOTE 1 —————

If the NAV-750 END lamp lights at the band-stop frequencies of 117.950, 135.975, or 157.950 MHz, the channeling will stop and the COMM-760 will revert to STANDBY mode. Continue channeling by setting the thumbwheel switches to the next desired channel.

————— NOTE 2 —————

The modulation frequency is restricted to 1020 \pm 5Hz since a notch filter is used to develop the noise-only component of the quotient.

In TONE V (Tone Oscillator Voltage Level) position, the tone level to the U.U.T. transmitter's microphone input can be measured at either 1 or 10 volts full scale.

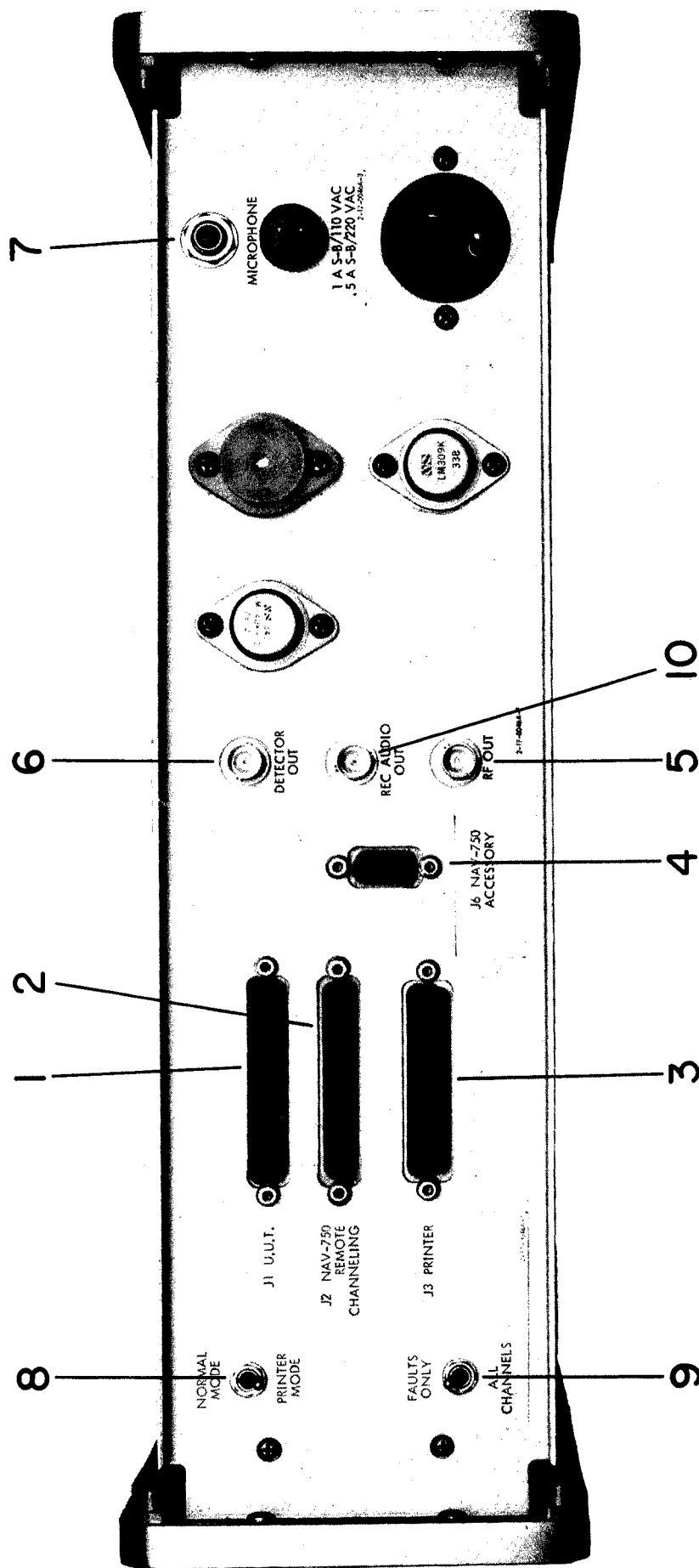
4. 1V/10V. Selects either 1 volt or 10 volt full scale sensitivity for the left hand meter in its RCVR V or TONE V function.
5. 1020/VAR. Selects either a fixed (1020Hz) or variable frequency for the test set's tone oscillator.
6. HIGH/LOW. Selects either the High (0.575-13 kHz) or Low (0.150-3.3 kHz) frequency range for the variable tone oscillator.
7. TONE FREQ. Varies the frequency of the test set's tone oscillator.
8. TONE LEVEL. Varies the tone oscillator level to the U.U.T. transmitter's microphone input. This level is measured by the left hand meter if its function switch is in the TONE V position.
9. OVER MOD. When lighted, indicates that the U.U.T. transmitter's negative peak modulation has exceeded an internally adjustable limit, nominally 98%.
10. MEASURE/SET LIMIT (Volts). Used with the RCVR V Position of the meter switch. In MEASURE, the voltmeter measures the U.U.T. receiver's audio output voltage. In SET LIMIT, the meter displays the fault decision level. This level can be varied with the control just right of the switch. The fault sensing circuitry operates even though the switch is in the SET LIMIT position.
11. NAV-750 EXT MOD/OFF. The switch connects or disconnects a fixed-level output of the test set's tone oscillator to the NAV-750's external modulation input. The fixed level modulates the NAV-750 to 30% AM when its MASTER MOD control is in the detented (calibrated) position.
12. VOL (Volume). Adjust the output level of the amplifier/speaker connected to the U.U.T. receiver's audio output.
13. POWER Meter. Measures the RF power of the U.U.T.'s transmitter on the 100W scale.

14. MEASURE/SET LIMIT (Power). In MEASURE the meter measures the U.U.T.'s transmitter power. In SET LIMIT, the meter displays the fault decision level. This level can be varied with the control just left of the switch. The fault sensing circuitry operates even though the switch is in the SET LIMIT position.
15. XMTR KEYED. When lighted, indicates that the U.U.T.'s transmitter is keyed.
16. PUSH TO XMIT. In STANDBY mode, pushing this button keys the U.U.T.'s transmitter for 3 seconds. In OPERATE mode, pushing the button starts the channeling again if the action had been stopped because any of the fault lamps were lit or in going from STANDBY to OPERATE mode when the printer is used.
17. XMIT TIME. Controls the time the U.U.T.'s transmitter is keyed during automatic channeling operation. The transmit/receive duty cycle is 40/60 for any selected transmit time.
18. RCVR, POWER, FREQ Fault Lamps. When lighted, indicates that the parameter is outside the selected limits. In NORMAL mode operation (selected on back-panel NORMAL/PRINTER mode switch) if any parameter has faulted, that fault lamp will light and NAV 750 channeling will stop. If the POWER or FREQ lamps light, the channeling can be continued by pushing the NAV-750 STEP and COMM-760 button. If the RCVR lamp lights, the channeling will begin again when the fault sensing circuitry measures a "no-fault" condition even if just for an instant. This means that if the Receiver's S + N/N or output voltage is just at the 6dB or voltage decision level, the noise component of the measurement causes the RCVR lamp to blink, and the first time the lamp blinks out a "no fault" signal is generated. This condition is the result of a compromise between the time required to average this noise measurement at the Test Set's fastest channeling rate.
19. ON/BYPASS SWITCHES. In ON, the RCVR, POWER, and FREQ fault lamps operate as in paragraph 18. In BYPASS, a no-fault condition can be simulated for any parameter thus bypassing that test. If all three switches are placed in BYPASS, the Test Set reverts to STANDBY mode.

20. AUDIO/RF. In AUDIO, the frequency counter measures the Test Set's audio oscillator frequency with a resolution of 1 Hz and gating time of one second. This position also places the Frequency Fault system in bypass mode since the counter is normally used to measure the U.U.T.'s transmitter frequency.
- In RF, the frequency counter measures the U.U.T.'s transmitter frequency with a resolution of 0.1 kHz and gating time of 0.1 second.
21. FREQUENCY - MHz Readout. In AUDIO mode, measures the frequency of the test sets audio oscillator with a resolution of 1Hz and gating time of one second. In RF mode, the frequency counter measures the U.U.T.'s transmitter frequency in MHz with a resolution of 0.1 kHz and a gating time of 0.1 seconds. A second decimal point is provided at the kHz position to facilitate readings down to tenth's of kHz.
22. FREQUENCY ERROR - kHz Readout. Measures the difference between the NAV-750 commanded frequency and the U.U.T.'s transmitter frequency. Maximum error measured is ± 19.9 kHz.
23. ERROR LIMIT - kHz. Selects the decision level for the Frequency Error Fault System. Maximum setting is 9.9 kHz.
24. NAV-750 RF. For incoming RF from NAV-750. There is a 20dB loss from here to the ANT connector.
25. ANT. Coaxial connector for antenna line on U.U.T. (See Note 3)

————— NOTE 3 —————

Maximum transmitter input is 30W at 50% duty cycle and 100W at 15% duty cycle or 15W CW (Uninterrupted). The ON time is 10 seconds maximum at 100W, 20 seconds at 50W, and 2 minutes at 30W.



REAR PANEL CONNECTORS
AND CONTROLS

FIG. 3-2

3-17. Functional Description of Rear Panel Connectors and Controls. (See Fig 3-2)

- ① U.U.T. - J1. (Back Panel) Connector for 2-out-of-5 line channel programming, audio input and output, and push-to-talk lines from U.U.T.
- ② NAV-750 REMOTE CHANNELING - J2. (Back Panel) Connector for 2-out-of-5 and BCD channel programming from NAV-750.
- ③ PRINTER - J3. (Back Panel) Connector for channel frequency and frequency error BCD lines, fault signals, and printer controls to external digital printer.
- ④ NAV-750 ACCESSORY - J6. (Back Panel) Connector for NAV-750 External Modulation and Channel Advance inputs.
- ⑤ RF OUT (-40 dBc, 50 ohm) - J20. (Back Panel) Output connector for oscilloscope viewing of U.U.T.'s transmitter signal. Signal is attenuated 40dB and should be terminated at the oscilloscope with 50 ohms.
- ⑥ DETECTOR OUT - J21. (Back Panel) Output from AGC Detector for oscilloscope viewing of U.U.T.'s transmitter modulation. The detected carrier corresponds to a DC level of approximately -2.2V for RF inputs of 4 to 100W.
- ⑦ MICROPHONE - J22. Connector for microphone used to modulate U.U.T.'s transmitter.
- ⑧ NORMAL/PRINTER MODE. (Back Panel) In NORMAL mode (external printer not used), when a POWER or FREQUENCY fault lamp lights, the NAV-750 channeling stops. The channeling can be continued by pushing the PUSH TO XMIT button. If the RCVR lamp lights, the channeling will begin again when the fault sensing circuitry measures a "no-fault" condition even if just for an instant. In this mode, fault determination for transmitter parameters is made at the end of the selected transmit time to allow the U.U.T.'s transmitter output power and frequency to settle. The receiver fault determination is continuously made subject to the conditions in paragraph 18.

In PRINTER MODE, printer control signals are generated that allow a printout of channel frequency, U.U.T.'s transmitter frequency error, and status of the three fault lamps ("1" for lamp off, no-fault condition; "0" for lamp on, fault condition). In this

mode channeling does not stop if a fault occurs. The timing sequence is as follows: after U.U.T. RCVR, POWER, and FREQUENCY tests for one channel have been made, a print command is generated. The printer's Inhibit or Busy signal prevents a channel advance signal from being sent to the NAV-750 until the printer cycle is completed. When the Inhibit or Busy line indicates that the printing has finished, a channel advance signal is sent to the NAV-750 and the measurement cycle repeats. Note that the printer time is added to the cycle time making the measurement cycle rate approximately .75 channel/sec maximum compared to approximately 1 channel/sec maximum in NORMAL mode. In this mode fault determination for both receiver and transmitter parameters is made at the end of each mode's allotted time.

- ⑨ ALL CHANNELS/FAULTS ONLY. In ALL CHANNELS, the print command is generated for each channel whether a fault has been detected or not. In FAULTS ONLY, only those channels with at least one fault will be listed on the printer.
- ⑩ REC AUDIO OUT - J32. (Back Panel) Output jack connected to U.U.T.'s receiver audio output enables distortion analyzer or other instruments to easily be connected to the U.U.T.

TABLE 3-1

J1 Unit Under Test (U.U.T.) Connector

1. 1 MHz C	28. n.c.	
2. 1 MHz B	29. n.c.	
3. 1 MHz A	30.	
4. 10 MHz E	31.	Do not use
5. 10 MHz D	32.	
6. 10 MHz C	33.	
7. n.c.	34. n.c.	
8. 10 MHz A	35.	Do not use
9. 10 MHz B	36.	
10. .01 MHz B	37. n.c.	
11. Common 2 of 5		
12. .01 MHz C		
13. .01 MHz D		
14. .01 MHz E		
15. BCD GND		
16. P.T.T.-1		
17. Rec GND		
18. Rec Audio Output		
19. Trans Mic Input		
20. .01 MHz A		
21. .1 MHz E		
22. .1 MHz D		
23. .1 MHz C		
24. .1 MHz B		
25. .1 MHz A		
26. 1 MHz E		
27. 1 MHz D		

Pin No

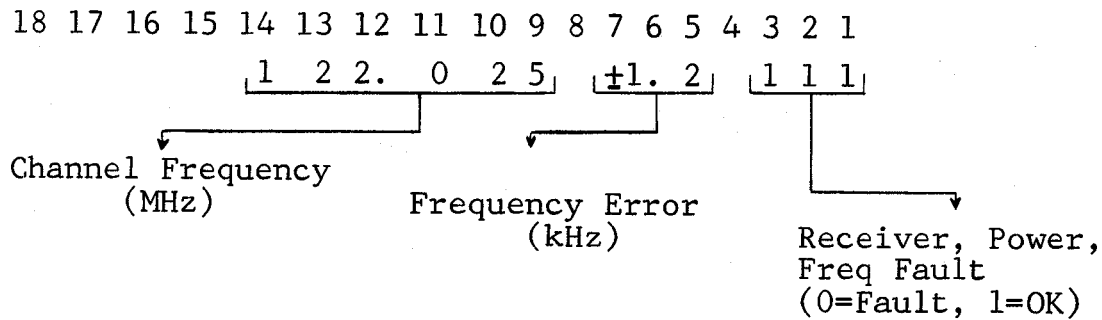
1	<u>Frequency Fault B</u>
2	<u>Power Fault B</u>
3	<u>Receiver Fault B</u>
4	n.c.
5	n.c.
6	n.c.
7	n.c.
8	n.c.
92 MHz
10	n.c.
11	n.c.
1205 MHz
13	4 MHz
14025 MHz
15	1 MHz
16	20 MHz
17	n.c.
18	1 KHz F.E. (Frequency Error)
19	2 KHz F.E.
20	4 KHz F.E.
21	8 KHz F.E.
221 KHz F.E.
232 KHz F.E.
244 KHz F.E.
258 KHz F.E.

TABLE 3-2 contd

J-3 Printer Connector Cond

<u>Pin No</u>	
264 MHz
27 n.c.
28 n.c.
29 40 MHz
30 2 MHz
318 MHz
32 8 MHz
33 10 MHz
34 n.c.
35 n.c.
36 n.c.
37 Faults Out
38 <u>Printer Inhibit In</u>
39 <u>Printer Inhibit In</u>
40 <u>Printer Inhibit Out</u>
41 <u>Print Command</u>
42 <u>Print Command</u>
43 (+) Print
44 (-) Print
451 MHz
46 n.c.
47 n.c.
48 n.c.
49 n.c.
50 GND

TABLE 3-3

Typical Printer FormatCOLUMNTYPICAL ± PRINTER DRIVEPRINTER TYPEDISPALYBCDDRIVENewport 810:

+	1010	BCD 8 hardwire Logic 1
-	1100	BCD 1 hardwire Logic 0
		BCD 2 to J3-43 (+ print)
		BCD 4 to J3-44 (- print)

HP 5055A:

+	1010	BCD 8,2 hardwire Logic 1
-	1011	BCD 4 hardwire Logic 0
		BCD 1 to J3-44 (- print)
		J3-43 (+ print) (not used)

TABLE 3-4
COMM-760/NAV-750
INTERCONNECTION CABLES

COMM-760 J6 (9 Pins) <u>"NAV-750 Accessory"</u>		NAV-750 J10 (15 Pins) <u>"Accessory"</u>	
(EXT MOD)	1	(EXT MOD)	11
(STDBY)	8	(END CH)	12
(FREQ ADV)	9	(REM CH)	6

COMM-760 J2 (37 Pins) <u>"COMM-760 Freq Programming"</u>		NAV-750 J8 (37 Pins) <u>"Remote Channeling"</u>	
(1 MHz C)	1	1	1
(1 MHz B)	2	2	2
(1 MHz A)	3	3	3
(10 MHz E)	4	4	4
(10 MHz D)	5	5	5
(10 MHz C)	6	6	6
(N.C.)	7	7	7
(10 MHz A)	8	8	8
(10 MHz B)	9	9	9
(.01 MHz B)	10	10	10
(2 of 5 COM)	11	11	11
(.01 MHz C)	12	12	12
(.01 MHz D)	13	13	13
(.01 MHz E)	14	14	14
(BCD GND)	15	15	15
(.05 MHz)-BCD	16	16	16
(.1 MHz)-BCD	17	17	17
(N.C.)	18	18	18
(.2 MHz)-BCD	19	19	19
(.01 MHz A)	20	20	20
(.1 MHz E)	21	21	21
(.1 MHz D)	22	22	22
(.1 MHz C)	23	23	23
(.1 MHz B)	24	24	24
(.1 MHz A)	25	25	25
(1 MHz E)	26	26	26
(1 MHz D)	27	27	27
(10 MHz)-BCD	28	28	28
(20 MHz)-BCD	29	29	29
(40 MHz)-BCD	30	30	30
(8 MHz)-BCD	31	31	31
(1 MHz)-BCD	32	32	32
(.8 MHz)-BCD	33	33	33
(.025 MHz)-BCD	34	34	34
(2 MHz)-BCD	35	35	35
(4 MHz)-BCD	36	36	36
(.4 MHz)-BCD	37	37	37

Transceiver Testing Procedures

3-17. Introduction.

3-18. The remainder of this section contains procedures for performing typical transceiver tests using the test set and a NAV-750 Signal Generator. Other tests can be developed using the guides contained here covering the positions of COMM-760 and NAV-750 controls and switches. Some examples: a check on the receiver's compressor could be made with the same control settings as those in Paragraph A.1 for manually measuring receiver audio output levels; or transmitter distortion measurement could be made with control settings as in paragraph B.3 using the back panel DETECTOR OUT connector.

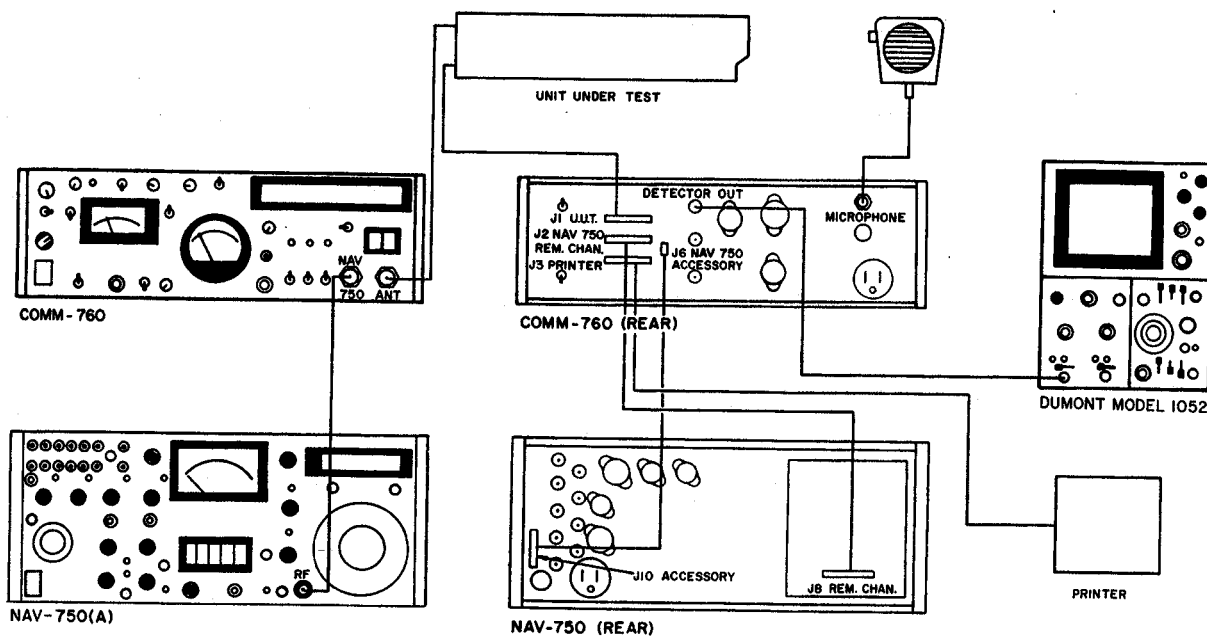


Figure 3.3
Equipment Setup

3-19. Operating Instructions.

- I. Manual Mode: Begin each Manual Mode test with the following settings except as indicated in specific tests.

COMM-760

STANDBY/OPERATE. STANDBY
Meter Function Switch. . . RCVR V or S+N/N as desired
SET LIMIT/MEASURE Switch . SET LIMIT (IF RCVR V
(Volts) chosen above)
SET LIMIT Control. Desired receiver audio
(Volts) output voltage fault
decision level.
1V/10V As required above.
NAV-750 EXT MOD. OFF
SET LIMIT/MEASURE Switch . SET LIMIT
(Power)
SET LIMIT Control. Desired Transmitter
(Power) power fault decision level
ON/BYPASS ON (all three)
AUDIO/RF RF
ERROR LIMIT - kHz. Desired transmitter frequency
error fault decision level

PRINTER

Power. OFF

NAV-750

BEARING/FREQ FREQ
1020Hz CAL (Full ccw, in detent)
MASTER MOD CAL (Full ccw, in detent)
AUTO/MANUAL. MANUAL
F. CAL (Full ccw, in detent)
FREQUENCY. Desired Frequency
RF Attenuator. Desired RF level plus 20dB

A. Receiver Test. (Place SET LIMIT/MEAS to MEAS)

1. Receiver audio output. Place meter function switch to RCVR V and 1V/10V to appropriate range. Select desired RF level on NAV-750. The meter indicates the 1020Hz (or Noise) signal level across 500 ohms at the receiver output due to the 30% modulated RF input.
2. Signal-plus-Noise-to-Noise Ratio. Place meter function switch to S+N/N. Select desired RF level on NAV-750. The meter indicates the

S+N/N at the receiver output due to the 30% modulated RF input.

3. Frequency Response. Set Controls:

COMM-760

NAV-750 EXT MOD.ON (up position)
1020/VARVAR
AUDIO/RFAUDIO
Meter Function Switch.RCVR V
HI/LO (tone frequency range)as required

NAV-750

1020HzUNCAL, 0 (ccw,
but not in detent)
RF Attenuator.Desired RF level

Adjust TONE FREQ until digital display reads approximately 1 kHz and note the voltmeter reading as a reference point. Adjust TONE FREQ until voltmeter reads 3dB below reference point for both high and low frequency ends of the band.

B. Transmitter Tests (Place SET LIMIT/MEAS to MEAS)

1. Power. Press PUSH TO XMIT button. Transmitter will continue to be keyed for approximately 3 seconds after the button is released. The POWER meter indicates the transmitter power on the 0-100 Watt scale.
2. Frequency. Press PUSH TO XMIT button. FREQUENCY digital display indicates transmitter frequency and FREQUENCY ERROR display indicates transmitter frequency error.
3. Modulation Sensitivity. Place Meter Function Switch to %MOD. Select the desired frequency using the 1020/VAR, HI/LOW, TONE FREQ, and AUDIO/RF controls. Adjust TONE LEVEL for desired peak modulation reading on meter when PUSH TO XMIT is pressed. Place Meter

Function Switch to TONE V and read the tone level at the transmitter's microphone input.

NOTE

The demodulated carrier output on the back panel, DETECTOR OUT, can be used to check the transmitter's waveform.

The detected carrier corresponds to approximately -2.2V. There is a slight (approx $\pm .2V$) bias on the detector diode, and this level is the reference point for 100% negative peak modulation. The RF output jack at the back panel used to display the carrier envelope is attenuated 40dB \pm 3dB from the carrier and should be terminated at the oscilloscope in 50 ohms.

II. Automatic Channeling Modes.

- A. NORMAL Mode: Begin each Automatic Mode test with the following settings except as indicated in specific tests.

COMM-760

STANDBY/OPERATE.	STANDBY
Meter Function Switch. . .	RCVR V or S+N/N as desired
SET LIMIT/MEASURE Switch .	SET LIMIT (IF RCVR V
(Volts)	chosen above)
SET LIMIT Control.	Desired receiver audio
(Volts)	output voltage fault
	decision level.
1V/10V	As required above
NAV-750 EXT MOD.	OFF
SET LIMIT/MEASURE Switch .	SET LIMIT
(Power)	
SET LIMIT Control.	Desired transmitter power
(Power)	fault decision level
ON/BYPASS.	ON (all three)
AUDIO/RF	RF
ERROR LIMIT kHz	Desired transmitter
	frequency error fault
	decision level.
NORMAL/PRINTER MODE. . . .	NORMAL MODE

PRINTER

Power. OFF

NAV-750

BEARING/FREQ. FREQ
1020Hz. CAL (Full ccw, in detent)
 Δ F CAL (Full ccw, in detent)
FREQUENCY Desired start frequency
200/100/50/25 kHz Desired channel spacing
MANUAL/AUTO AUTO
CHANNELING INC RATE Fully ccw
RF Attenuator Desired RF output plus 20dB

When all fault decisions levels have been set up, place STANDBY/OPERATE to OPERATE. The test set will immediately start to measure the receiver and transmitter parameters at a rate selected by the XMIT TIME control, and the NAV-750 annunciator will sound each time a new channel is being checked.

When any parameter falls outside the selected limits, the channeling will stop and the fault lamp will light.

NOTE

If POWER or FREQ lamps light, the fault is "stored", the transmitter will stay keyed for 3 seconds, and channeling stops. However, the RCVR lamp will light and the channeling will stop only as long as a receiver fault measures right at the fault decision level. The RCVR fault lamp may flicker, due to noise, before a passing measurement is made and channeling is continued.

To continue channeling after a POWER or FREQ fault press the NAV-750 STEP button to advance to the next channel, then press PUSH TO XMIT. If the NAV-750 END lamp lights at the band-stop frequencies of 117.950, 135.975, or 157.950 MHz, the channeling will stop and the COMM-760 will revert to STANDBY mode. Continue channeling by setting the thumbwheel switches to the next desired channel.

- B. PRINTER Mode: Set controls as in IIA on page 3-16 except the following back panel controls:

NORMAL/PRINTER MODE. PRINTER MODE
FAULTS/ALL CHANNELS. As desired

PRINTER

Power.ON

The PRINTER MODE operation is identical to NORMAL mode as shown on page 3-20 except that the printer records the test results for each channel (ALL CHANNELS selected), or only those channels that have at least one fault (FAULTS ONLY selected). The channeling rate will be slightly slower due to addition of the printer's cycle time to the total channeling time.



SECTION IV

Theory of Operation

4-1. Introduction.

4-2. This section contains first an overall explanation of the Test Set operation using the block diagram of Figure 4-1 as a guide and then a detailed description of each circuit using the schematics of Section IX as a guide.

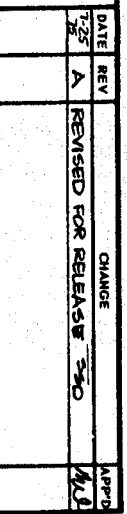
4-3. Test Set Block Diagram. Refer to Fig 4-1.

4-4. The two connections between the Unit-Under-Test (U.U.T.) and the Test Set are the J-33, ANT, and J1, U.U.T., connections. The J-33 ANT connector acts as an input for the U.U.T.'s transmitter output and an output for the NAV-750 Signal Generator signal to the U.U.T.'s receiver. The 20dB power attenuator between the ANT and NAV-750 RF connectors absorbs the U.U.T.'s transmitter power, and 20dB must be subtracted from the NAV-750 output when making U.U.T. receiver sensitivity measurements. The ANT signal is also coupled at a 40dB reduced level to the back panel RF connector (-40dBc) used for spectrum analyzer or oscilloscope displays of the U.U.T. carrier. A second 40dB down sample of the ANT signal feeds the Prescaler and AGC Detector Modules. Both couplers are formed by a 5K ohm resistor connected directly to the center conductor of the Bird Corp "ThruLine" Power Detector Module. The Detector Module contains the directional, plug-in detector element whose output is amplified on the Main Circuit Board and displayed on the POWER meter.

4-5. The sample of the U.U.T.'s transmitter connected to the AGC Detector produces a detected output which is constant for carrier level of about 2 watts to above 50 watts. This detected output is peak detected on the Main Circuit Board for display on the % Modulation meter and the back panel DETECTOR OUT connector. The AGC Detector also contains an RF buffer whose output is connected to the $\div 10$ Prescaler.

4-6. The Main Circuit Board is divided into two main sections —the Timer section and the Measurements section. The timer section controls the timing for cycling of the test set between the receiver and transmitter measurement modes and contains logic for the fault display system. Commands for the external printer are also generated in this section





4-1.1

17-0003	1	COMM-760	1	1	17-0032	BLOCK DIAGRAM
NEXT ASSY QTY	MODEL	ITEM REQ'D	PART NO.	DESCRIPTION		
APPLICATION					LIST OF MATERIALS	
TOLERANCES					INSTRUMENT FLIGHT RESEARCH CORPORATION	
UNLESS OTHERWISE SPECIFIED					WICHITA, KANSAS	
ALL DIMENSIONS APPLY AFTER FINISH					TITLE	
REQUIREMENTS: 2 .006					BLOCK	
ANGLES: 2 1/2°					DIAGRAM	
FRACTIONS: 2 1/8, 1/8					COMM-760	
PRACTICE DIMENSIONS					SIZE	
REMOVE ALL BURRS					B	
MATERIAL					SCALE	
TREATMENT					WELDED	
FINISH					SHEET 1 OF 1	
DRAWN DATE					APPROVED DATE	
JUN 1-57					7-5-74	
CHECKED DATE					APPROVED DATE	
MJD 7454						

- 4-7. The Measurement section contains circuitry for signal-plus-noise and voltage measurements, a tone oscillator, and comparators that signal the timer section when the measured parameters fall below the adjustable or fixed test limits.
- 4-8. The frequency counter system counts either the prescaled sample of the U.U.T.'s carrier or the Test Set's tone oscillator.
- 4-9. The frequency error counter displays the difference between the frequency programming from the NAV-750 and the counted frequency of the U.U.T. The frequency programming BCD information and the frequency error information are available at the printer connector as are a "1" or a "0" for fault lamp status for receiver, transmitter power, or transmitter frequency measurements.
- 4-10. Detailed Circuit Description.
- 4-11. AGC Detector. (Refer to Fig 9-6)
- 4-12. A sample of the U.U.T.'s transmitter signal attenuated by 40dB is connected to J-16. This sample is then connected to the $\div 10$ prescaler via buffer amplifier Q-302. The sample is further attenuated by R303/304 and passes through a current controlled attenuator, pin diode CR301. The signal is then amplified by Q303-305 and detected at CR305. The feedback loop amplifier, X302, varies the current through (and thus RF attenuation of) CR301 until the detected carrier level at C319 is approximately -2.2V, the 12V reference multiplied by the ratio of R315 to R314. The point at which the AGC lamp just begins to cut-in is determined by the select-at-test resistor R304. Its value is chosen so the loop just begins to respond when -10 dBm RF power is present at J-16 (-10 dBm at J-16 corresponds to a 1W carrier level at the front panel ANT jack), L309 tunes out some capacitance of CR305 and Q305 at the upper end of the band.
- 4-13. The AGC detector output is a constant dc level of approximately -2.2V with an ac component proportional to the modulation level of the U.U.T.'s transmitter. The positive going peaks of this signal which correspond to negative modulation are then peak detected by X233 on the Main Circuit board and displayed on the front panel meter.

- 4-14. Power Meter Circuits. (Refer to Fig 9-1)
- 4-15. The Bird "Thruline" detector output at P11-1 is loaded by R252 to simulate the 30uA meter movement that is normally connected directly to the detector output. The detector signal is then amplified by a factor of 51 at the output of X219A and connected to the meter movement and the power fault comparator, X219B. The amplifier is necessary to prevent the transients across the meter movement terminals from affecting the comparison of the measured power level to the fault decision level set into R805, SET LIMIT (power). The comparator output is high when the measured power is lower than the decision limit power level.
- 4-16. Tone Oscillator. (Refer to Fig 9-1)
- 4-17. X221 is a voltage controlled function generator whose frequency is controlled by the dc level at R811, TONE FREQ, in VAR mode with C236 for the LOW frequency range. The square wave output at X221-9 is connected to the frequency counter and the sine wave output at pin 2 is connected to buffer amplifier X222. The buffer's output is used to modulate the NAV-750 Signal Generator to approximately 30% AM. X220 is used as a power amplifier to drive the low impedance microphone input on the U.U.T. The tone oscillator signal is connected to the microphone input only when S805, Meter Function switch is in either the % MOD or TONE V positions. J22, MICRO PHONE, is also connected to the U.U.T. and allows the transmitter to be keyed by an external microphone which energizes the push-to-talk relay, K201 (Timer Section, Fig 9-4).
- 4-18. Voltmeter. (Refer to Fig 9-2)
- 4-19. Inputs to the ac voltmeter circuit come from the U.U.T.'s receiver audio output (loaded with 500 ohm resistor, R801) or the tone oscillator. R2041/2043 attenuate these signals to prevent X1/X10 gain buffer X223B from being over driven by 10V rms sine waves. With S801, 1V/10V, in the 10V position, X223B is connected as a gain of one buffer. With S801 in the 1V position, R2042/277 are grounded making X223B a gain of 10 buffer.
- 4-20. X223A/224B form a fullwave rectifier. When the input signal is positive, X223A output is driven negative to -0.7V (CR224 is a clamp) and CR223 is reverse biased.

Thus X224B becomes a gain of plus one buffer and the output at pin 7 is positive (same polarity and magnitude as input). When the input signal is negative, X223A is driven positive and CR223 turns on. Since R279 and R280 are equal, X223A's summing junction will only be satisfied when the X224B output is equal but opposite polarity to the input signal. This is accomplished by the output of X223A forcing X224B output to the correct level.

- 4-21. The output of the full wave rectifier is displayed on the front panel meter via R1403/1404. The rectifier output is averaged by R2032 and C269 and connected to voltmeter fault level comparator X224A. The second comparator input is the dc level from R803, SET LIMIT (volts).
- 4-22. Signal + Noise-to-Noise-Ratio Circuits. (Refer to Fig 9-2)
- 4-23 The measurement is made by forming a dc level proportional to signal-plus-noise (V_{S+N}) and a second proportional to noise only (V_N). An analog divider is then used to take the ratio.
- 4-24. A sample of the receiver's audio signal is connected to audio AGC amplifier, X225A/Q215, whose output is approximately 3.7V rms for input levels of 0.1 to 10V rms. The use of the AGC amplifier before the ratio computation reduces the dynamic range requirement of the divider circuit. X225B/226A form an inverting full wave rectifier whose output after being filtered by C255 is $-V_{S+N}$. The AGC loop is closed by error amplifier X226B comparing the average value of $-V_{S+N}$ to the +12V supply. The error voltage controls the gate voltage and hence the drain-source channel resistance of Q215. R282 and Q215's channel form a variable attenuator at the input of the AGC amplifier.
- 4-25. The signal-plus-noise at the output of the AGC amplifier is connected to notch filter X227 which is tuned to reject the signal frequency of 1020Hz. The filter's 6dB bandwidth is 70Hz. X228 is a non-inverting full wave filter whose output after being filtered by C251 is $+V_N$.
- 4-26. Divider circuit X229/230B performs the ratio $-V_{S+N}/V_N$ with a gain of approximately 1.4 and an output at X230B pin 7. Trimpots P-1 through P-3 are adjustments for input and output offset voltages for divider IC X229. X230A is connected as a comparator to determine when the 6dB S+N/N fault decision level has been exceeded.

- 4-27. % Modulation Peak Detector. (Refer to Fig 9-2)
- 4-28. The detected transmitter output from the AGC Detector is connected to the input of positive peak detector X233 whose dc output equals the positive peak value of the dc input across R2022. Since the AGC Detector output is negative, positive going peaks correspond to negative modulation peaks. These peaks are stored across C258, buffered by X232B and displayed on the front panel meter. X232A is connected as a comparator to determine when the peak detector output has sensed overmodulation.
- 4-29. Clock Circuit. (Refer to Fig 9-3)
- 4-30. The 10 MHz crystal is mounted in an oven assembly which is powered by the 12V busses. The oven contains a solid state device which is low impedance until an interior temperature of approximately 85° C. is reached. At this temperature the impedance rises lowering the power dissipation and stabilizing the temperature. The oscillator transistor output at Q201 emitter is buffered by Q202 connected as an emitter follower and Q203. X201 and CR201 form an automatic level control feedback loop which regulates the signal at Q202's emitter to approximately 1.2V P-P by controlling the emitter current through Q201.
- 4-31. Timer Circuitry. (Refer to Fig 9-4)
- 4-32. "Normal" Mode Timing. (Refer to Fig 4-2). With S802 in the "Normal" mode position, the chain of events in the timing section is:
- 1.) Assume S806 has just been moved from STANDBY to OPERATE. If REC FAULT A is high (signaling no-fault condition of the receiver voltage or S+N/N circuitry), and if the power or frequency fault lamps are not lit (PWR FAULT B and FREQ FAULT B both high), X207B-8 goes low and X207A-6 goes high. The positive going edge of the X207A-6 signal triggers X212A, MAX XMIT TIME one shot (O/S).
 - 2.) X212A keys the transmitter via K201, P.T.T. relay, and triggers X209, DELAY - XMIT to SAMPLE O/S. X209's time is controlled by R804, XMIT TIME. This X209 delay time allows the transmitter's power and frequency to stabilize, the frequency error counter to make its measurement, and allows the operator to read power and frequency during channeling (when XMIT TIME is rotated maximum cw).

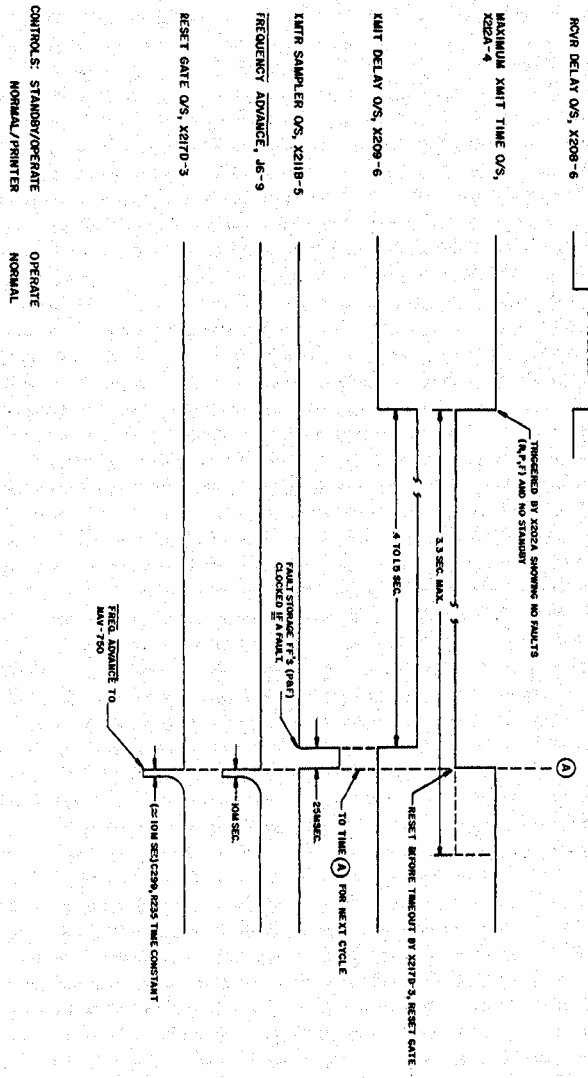
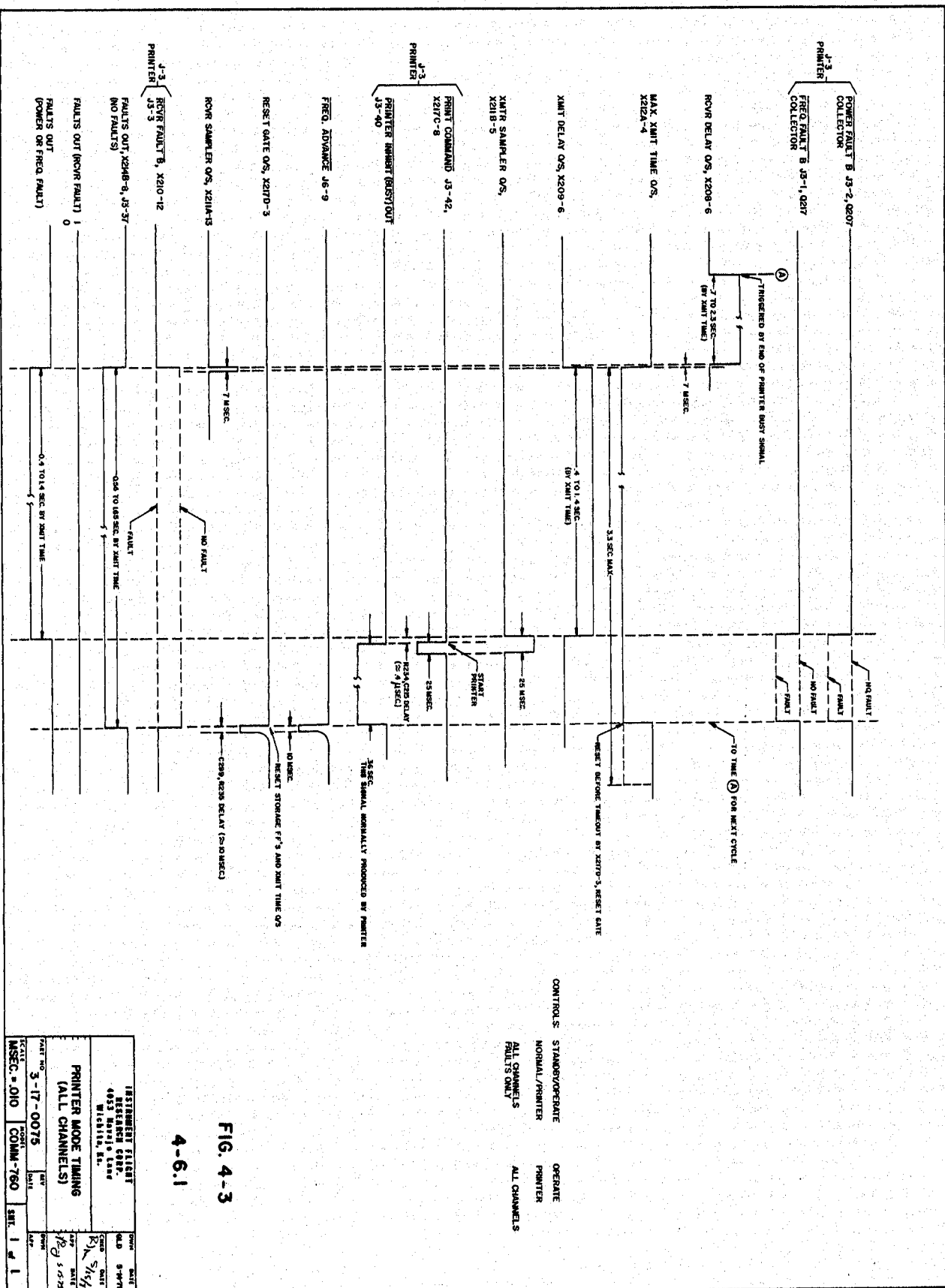


FIG. 4-2

4-5.1

INSTRUMENT FLIGHT		4853 Navy's base		4853 Navy's base	
MISSILE, etc.		MISSILE, etc.		MISSILE, etc.	
NORMAL MODE TIMING		3 - 17 - 0076		COMM-760	
SCALE NO.		3 - 17 - 0076		COMM-760	
MSEC. = 010		COMM-760		SRT. 1	
DATE		DATE		DATE	
BY		BY		BY	
CHECKED		CHECKED		CHECKED	
APPROVED		APPROVED		APPROVED	

- 3.) After X209 timeout, X211B, XMTR SAMPLER O/S, is triggered. This O/S prevents power or frequency fault signals from being clocked into the FAULT STORAGE flip-flops, X215B and X215A, until the end of the transmit mode time.
- 4-33. If no power or frequency faults have occurred, X214 pin 4 and 5 will be high and the XMIT SAMPLER pulse is inverted by X214A and triggers a O/S formed by X217A and R235/C299. The output of the O/S becomes the FREQUENCY ADVANCE signal to the NAV-750 to move to the next channel to be tested and also resets the MAXIMUM XMIT TIME O/S, X212A.
- 4-34. If a power or frequency fault has occurred during the time that XMTR SAMPLER O/S is active, the fault causes a 0 to appear on X211B pin 4 or 5 forcing pin 6 high and preventing the SAMPLER pulse from triggering X217D and advancing the NAV-750 frequency. The fault will also cause a 1 to appear on X216A-2 or X216B-5. This 1 allows the SAMPLER pulse to be inverted by X216A or X216B and clock FAULT STORAGE flip-flops X215B or X215A. If either flip flop has been clocked, its Q output is a 1 and the collector of Q207 or 217 is a 0. The 0 prevents another transmitter cycle from being started via the 0 at X207A pin 4/5 or 1. The fault lamps and the printer fault signals are also developed at the collectors of Q207 or Q217. When a power and frequency fault has occurred, X212A is allowed to time out (approximately 3.3 seconds) and causes the U.U.T. to stay keyed for this amount of time so the operator can look at the POWER meter or FREQUENCY display.
- 4-35. When a power or frequency fault has occurred, the fault can be cleared by pressing S804, PUSH XMIT. This triggers X212A, MAX XMIT TIME, via CR208 and clears X215B and X215A via CR218 starting another transmit cycle.
- 4-36. All Channels Printer Mode Timing. (Refer to Fig 4-3) The PRINTER MODE timing is similar to the NORMAL mode timing of paragraph 4-30 with the following exceptions: 1) the receiver fault is "sampled and stored" in a flip flop, 2) the receive mode on the next channel does not begin until after the printer has completed its cycle.
- 4-37. The cycle can be thought to begin when X208, DELAY-REC to SAMPLE O/S, is triggered by the previous cycle. After its timeout, X211A REC SAMPLER is triggered. For no receiver fault, X206C pin 10 is high and the sampler pulse



is inverted by X206C and clocks X210, REC FAULT STORAGE. If there is no receiver fault, the REC FAULT signal at X206C pin 10 is a 0 which prevents the sampler pulse from clocking X210.

- 4-38. The sampler pulse passes through X207B (if STANDBY/OPERATE is in OPERATE and if END OF CHANNELING is not true) and triggers X212A starting the transmit cycle. After X209 timeout, the XMTR SAMPLE O/S is triggered. If there are no power or frequency faults, the storage flip-flops are not clocked.
- 4-39. Approximately 0.4us after XMTR SAMPLER O/S is triggered a PRINT COMMAND is generated. When the printer has completed its print cycle, its inhibit or "busy" signal returns to the non-busy state triggering O/S X217D which resets the storage flip-flops and advances the NAV-750 frequency. (For printers with no inhibit output, X212B, PRINTER INHIBIT SIMULATOR O/S, is triggered by the PRINT COMMAND. The output of this O/S can be jumpered to the PRINTER INHIBIT INPUT in this case). The return of the PRINTER INHIBIT to the non-busy state also triggers X208A, REC to SAMPLE DELAY O/S, repeating the cycle at a new frequency.
- 4-40. Faults Only Printer Mode Timing. (Refer to Fig 4-3) The Faults Only mode timing is the same as the All Channel mode except that the Print Command is gated out at X217C for cycles where no fault is detected. The frequency of the NAV-750 is advanced every cycle by the "timeout" of X212B, PRINTER INHIBIT SIMULATOR, since in this mode X212B output is connected to perform reset gate and frequency advance functions.
- 4-41. RF/Audio Frequency Counter. (Refer to Fig 9.5.1)
- 4-42. With S814, RF/AUDIO, to RF, the counter counts the sample of the U.U.T.'s transmitter that has been prescaled by 10. At X711C pin 8 the square wave output from the prescaler has been reformed into narrow width spikes by the spiker circuit X712B, X711A, X711D, and X710C.
- 4-43. At X710B, the input frequency is "gated" by the 1 level of the clock (5Hz at X715A pin 6). X715B forms the $\div 2$ "front end" of the first decade counter with X419 being the $\div 5$ section. The BCD output from each counter is connected to a 4-bit latch, X411 through X416. X403 through X408 are decoder-drivers for the gas discharge readouts.

- 4-44. At the negative transition of the clock signal at X715A pin 6, the input pulses are gated out at X710B pin 6. The clock transition also fires O/S C713/R716/Q702. The positive going edge of Q702 collector signal strobes (latches) the count into the SN7475's and the negative going edge strobes X716A, the $\frac{1}{2}$ digit latch for the 100 MHz $\frac{1}{2}$ digit counter X716B.
- 4-45. The negative going edge of the Q702 collector signal also triggers O/S C714/R718/Q701. Q701's collector positive going edge resets the SN7490 and X716B and X715B counters. There is a slight delay (approximately 1us) from the Q702 negative going trigger signal to the Q701 positive going reset signal via the R719/C715 time delay.
- 4-46. With RF/AUDIO to AUDIO, the clock frequency is further divided by 10 at X703 and SPDT switch X709A pin 3. The clock frequency at the output of X715A pin 6 is now 0.5Hz. The audio tone oscillator square wave at P12-9 is now connected to the "gate", X710B, via X712D, X711C, and X710D.
- 4-47. Clock dividers X704 and X703 are reset to 9 at the end of the counting period by the 1 level pulse at Q702's collector. This shortens the time in between counts making the counter sequence 0 through 10 (counting time) and then 9-10 (reset-strobe time).
- 4-48. Frequency Error Counter. (Refer to Fig 4-4,4-5, and 9-5)
- 4-49. The Frequency Error Counter system displays the difference between the NAV-750 frequency and the frequency of the U.U.T.'s transmitter. This is accomplished by loading the programmable counter with the BCD words corresponding to the NAV-750 frequency command. These counters then count down towards zero at a rate determined by the prescaled transmitter frequency. If zero has been reached before the clock generated "gate" time ends, the transmitter frequency is higher than the NAV-750 frequency. A separate frequency error counter then counts the transmitter pulses from the time the zero count in the programmed counter was first detected to the end of the gate time. These counts are then displayed as positive frequency error.

$$[F_m > F_{MAN-750} + 0.5 \text{ KHz}]$$

$$[F_m = F_{MAN-750} + 0.5 \text{ KHz}]$$

FREQUENCY ERROR COUNTER TIMING

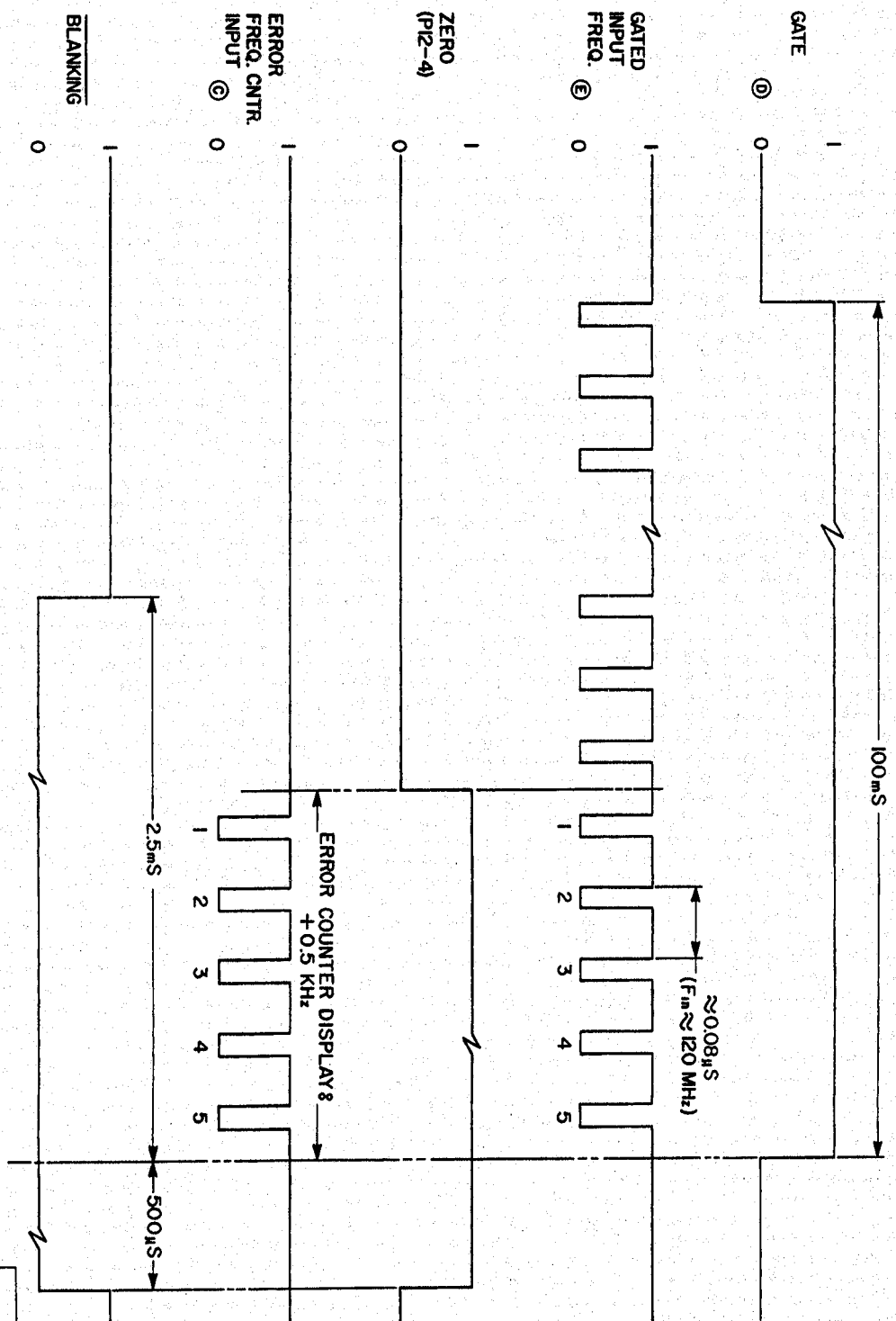


FIG. 4-4

4-9

INSTRUMENT FLIGHT		DATE
RESEARCH CORP.		6-29-75
4853 Nevada Lane		
Wichita, KS.		
FREQ. ERROR		DATE
COUNTER TIMING		6-29-75
TEST NO.	3-17-0077	REV.
SCALE	NONE	COMM-760
UNIT	SER.	1 of 1

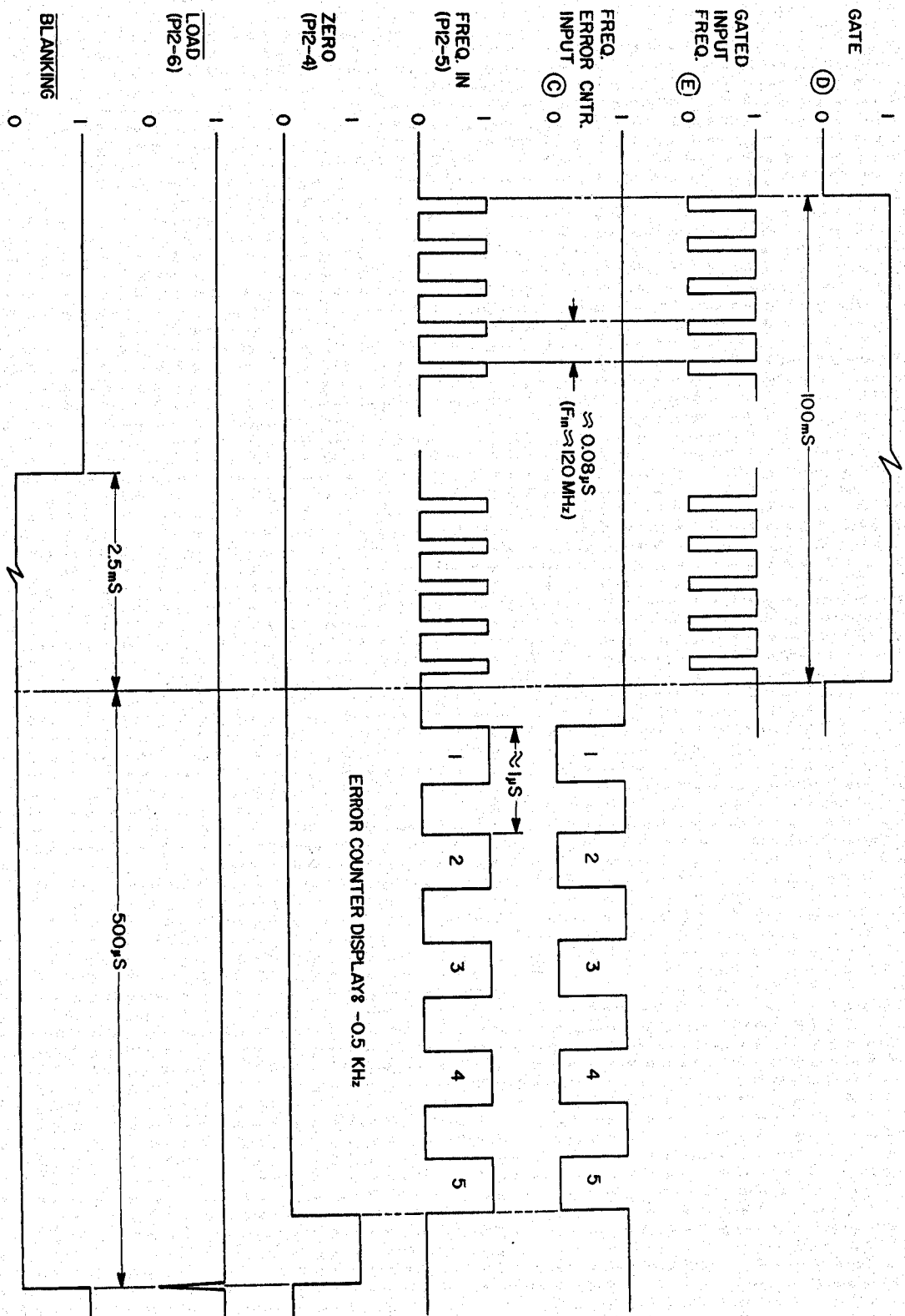


FIG. 4-5

4-10

$$[F_m < F_{MW-750} - 0.5 \text{ KHz}]$$

$$[F_m = F_{MW-750} - 0.5 \text{ KHz}]$$

FREQUENCY ERROR COUNTER TIMING

TESTMENT FLIGHT			
RESEARCH CORP.			
4050 Nevada Lane			
Wichita, KS.			
PART NO. 3-I-0078		REV.	DATE
FREQUENCY ERROR			
COUNTER TIMING			
SCALE	UNIT	SCALE	UNIT
NONE	COM-750	REL. 1	1

- 4-50. For the case of a transmitter frequency being lower than the NAV-750 frequency, the programmed counters do not reach zero count before the gate time ends. After the gate "closes", the counters are counted down to zero by an auxiliary pulse oscillator which is activated at the gate closure. The frequency error counter then counts the number of pulses necessary to reduce the programmed counter count to zero and displays the count as negative frequency error.
- 4-51. Detailed Circuit Description. (Refer to Fig 4-4 and 9-5)
- 4-52. The gated input pulses at point E are the prescaled transmitter pulses that have been "anded" with the 5Hz gate at the RF/Audio Frequency counter. These pulses are connected via X717A to the clock line of the programmed counters, X501 through X506, on the Frequency Error Counter Board. For the case of the input frequency being too low, the pulse generator, X707A/B, is also connected to the programmed counters via X717A.
- 4-53. For the case of an input frequency higher than the NAV-750 frequency, the ZERO line comes true (1 level) before the fall of the gate signal at point D. (See Figure 4-4) The 1 level allows the gated input frequency to pass through X717B,C, and D to the error frequency counters. X409, X410, and X418. At the end of the gate time the input frequency pulses disappear and the frequency error counter holds the count of the number of pulses counted from the leading edge of the ZERO to the falling edge of GATE signal. At the fall of the GATE signal, 500 μ s, 0/S X702 is triggered. At its time out a negative LOAD pulse is generated at X708B to reload the programmed counters to the NAV-750 frequency command for the next gate cycle. The 330pf, C730, capacitor on the ZERO line delays the interconnection of the input frequency pulses to the error counter so that the pulse causing the programmed counters to reach zero will not be counted by the error counter, but the next pulse will be the first pulse counted.
- 4-54. Note that when the input frequency is too high, ZERO is at logic 1 before, during, and after the fall of the 5Hz GATE at point D. R704/CR703 form an "and" gate at which ZERO prevents the falling edge of GATE from clocking X714. Thus X714's \bar{Q} output does not change from the reset state, and this logic 1 forces a logic zero at X708A pin 1 which inhibits the auxiliary pulse oscillator, X707A/B.

- 4-55. When the input frequency is too low, the GATE falls to logic 0, but a zero count still has not been reached in the programmed counters and ZERO is logic 0. (See Fig 4-5). Now at the falling transition of GATE, X714 is clocked via CR703. X714 Q flips low and releases the inhibit on the pulse oscillator. Its pulses are connected to the programmed divider via X717A and also to the frequency error counter via X717B/C. The Gated Input frequency signal at point E resets high when the gate is closed, i.e., at logic 0. When zero count is reached in X501-506, the logic 1 at ZERO inhibits the pulse oscillator via X708A and stops the frequency error count. The LOAD pulse is generated 500us from the GATE 1-0 transition which resets X714 and reloads the programmed counters.
- 4-56. Since the actual fraction of a GATE cycle spent in incrementing the frequency error counter is small, the frequency error count is not latched, but blanked for the duration of the count. The count occupies a few hundred microseconds either side of the 1-0 transition of the GATE, and the BLANKING signal is developed 2.5ms before the GATE transition of GATE and combining with GATE at X707B. This signal is "anded" by X707C with the RF/AUDIO switch output, point K, to blank the frequency error readout when the audio tone is counted. X707C output is combined at X708C with the 500us pulse that follows the GATE 1-0 transition. Thus the blanking signal extends 2.5ms before the GATE closing and 500us afterwards.
- 4-57. At X417A/C, BLANKING also inhibits FREQ FAULT A (point J) from going to logic 1 (fault condition) during the blanking time. The drive for the + or - sign display is derived from the auxiliary pulse oscillator triggering the retriggerable one shot, X713. Pulses will appear on the low active A input and a logic 1 will appear at the high active B input only when: the input frequency is too low; the pulse generator is oscillating; and GATE is logic 0.
- 4-58. The 1-0 transition (beginning), of the BLANKING pulse resets the frequency error counter via X417B, and this reset line is also activated by the leading zero output of the RF Audio counter, point F, which is logic zero when the first three significant digits are zero on the RF counter display (i.e., when the transmitter is not keyed).

- 4-59. The FREQ FAULT A signal is developed by clocking flip-flop X418 each gate cycle if a fault has occurred. The ERROR LIMIT thumbwheel switch and diodes CR801-808 form two four input and gates. If a certain limit frequency has been selected on the thumbwheels and the frequency error counter counts up to or greater than that count, at the time the count first reaches the thumbwheel setting logic 1's will appear on X417D pins 12 and 13. This clocks X418 generating the FREQ FAULT A signal. X418 is reset at the beginning of the BLANKING pulse, —just before a new count is made.

SECTION V

Performance Check Procedure

- 5-1. Introduction.
- 5-2. The procedures in this section check the Test Set's electrical performance using the specifications of Table 1-1 as performance standards.
- 5-3. After each step, instructions are given to enter either a checkmark (), or the measured value (record data), in the Performance Check Procedure Data Sheet that appears at the end of this section.
- 5-4. Equipment required for the performance test is listed in Table 5-1, Recommended Test Equipment for Calibration and Performance Check.

TABLE 5-1
Recommended Test Equipment
Calibration and Performance Check

Equipment (Critical Specifications)	Typical Example
Dual Trace OscilloscopeHP-180A
Digital MultimeterFluke 8000A
RF Power Meter (118-156 MHz, 100W max)	.Bird 43A Wattmeter 100C Element (with factory calibration chart)
Audio Distortion MeterHP-334A
AC Voltmeter (Average responding with dB scale)	.HP-334A
NAV-750 NAV/COMM/ILS Signal Generator	.IFR, NAV-750 or NAV-750A
RF Frequency Counter (Time base aging: 3 parts in 10^7 per week at constant ambient temperature	.Transistor Special- ties Inc. 385-R
Audio OscillatorInterstate Electronics Corp F-51
VHF Signal Generator (-10 to +10 dBm, 118-156 MHz	.Texscan VS-50
VHF Transceiver.Collins VHF-20
AM Modulation Meter.Marconi 2300A

5-5. Control Settings.

- 5-6. Begin the procedure with the front and back panel controls in the position shown below:

COMM-760

STANDBY/OPERATE	STANDBY
ON/BYPASS	ON (all three)
NORMAL/PRINTER MODE	NORMAL (backpanel)
MEASURE/SET LIMIT (volts)	MEASURE
MEASURE/SET LIMIT (power)	MEASURE

5-7. Performance Check Procedure.

- 5-8. Remove the Test Set's top cover.

- 5-9. Power Meter. ($\pm 10\%$ fs, 20-100W with 100W element or 5-25W with 25W element, 118-156 MHz).

- 5-10. Connect the output of the "Thruline" RF Power Meter directly to the front panel ANT jack. Connect the antenna cable of the VHF Transceiver to the input of the RF Power Meter. With no RF power applied, verify that the COMM-760 power meter reads zero. ()

With RF power applied, record the Test Level reading on the "Thruline" RF power meter and the COMM-760 Power Meter reading over the frequency range of 118 to 156 MHz. (Record Data)

5-11. Tone Oscillator.

(Fixed: $1020 \pm 10\text{Hz}$, or Variable: 150Hz to 13 kHz; 0-1.8V rms into 100 ohm, 3% THD)

- 5-12. Place Meter Function switch to TONE V, TONE LEVEL fully cw, 1020/VAR to 1020, and HI/LO to LO. Connect a 100 ohm $\pm 10\%$ load resistor to J22-ring, MICROPHONE (back panel). Connect the Frequency Counter, DVM, and Distortion Meter across the load resistor. Measure the ac voltage, frequency, and distortion of the tone oscillator signal at 1020Hz. (Record Data)

- 5-13. Place 1020/VAR to VAR. Rotate TONE FREQ fully ccw (minimum frequency) and measure the voltage, frequency, and distortion across the load resistor. (Record Data)

- 5-14. Place HI/LO to HI and rotate TONE FREQ full cw (Maximum Frequency). Measure the voltage, frequency and distortion across the load resistor. (Record Data)
- 5-15. Connect the DVM to J6-1, NAV-750 Accessory. Set NAV-750 EXT MOD to the up (ON) position. Measure the ac voltage that is available to modulate the NAV-750 Signal Generator. (Record Data)
- 5-16. S+N/N Circuits. Set Meter Function to S+N/N. Connect the VHF Transceiver and NAV-750 Signal Generator to the COMM-760 according to Fig 3-3. ()
- 5-17. Connect the Distortion Analyzer to J-32, RECEIVER AUDIO (back panel). Set the Analyzer's FUNCTION switch to VOLTMETER. ()
- 5-18. With the NAV-750 FREQUENCY switch at 125.000 MHz and the 1020Hz control in the detent position, adjust the RF attenuator until the COMM-760 meter reads 4dB. Note the Analyzer reading in dBm (signal-plus-noise level). Adjust the 1020Hz out of detent but fully ccw and again note the Analyzer dBm reading (noise level). Subtract the two readings and record the difference as S+N/N Test Level. (Record Data)
- 5-19. Repeat paragraph 5-18 for S+N/N meter readings of 6, 8, 10, 12, and 15dB. (Record Data)
- 5-20. AGC Amplifier Check. Reduce the signal-plus-noise level to about 100mV by shunting the receiver audio output at the Analyzer input with a resistor. Repeat paragraph 5-18 with a meter reading of 6dB. (Disconnect Transceiver (Record Data)
- 5-21. Voltmeter. (0-1V and 0-10V into 500 ohm, 50Hz to 5 kHz; $\pm 3\%$ full scale).
- 5-22. Set Meter Function Switch to RCVR V and 1V/10V to 1V. Connect the Audio Oscillator and the DVM to J-32, RECEIVER AUDIO (back panel). With the Audio Oscillator frequency at 1 kHz, adjust the Oscillator's output for the values indicated on the data sheet and record the Test Set's meter reading. (Record Data)

- 5-23. With the oscillator frequency at 50Hz and level at 0.5V, record the meter reading. Repeat for 5 kHz.
(Record Data)
- 5-24. Place 1V/10V to 10V. ()
- 5-25. Adjust the oscillator level to 5.0V and take data at 50Hz and 5 kHz.
(Record Data)
- 5-26. % Modulation Meter. (0-95%, \pm 3% f.s., 300Hz to 3 kHz)
Set Meter Function switch to % MOD. Connect the VHF Signal Generator to J-16 (inside the Test Set; see Fig 9-10 for location). Use the Modulation Meter to adjust the Signal Generator for a +3 dBm signal (corresponds to a 20W transmitter at the ANT jack) at 125 MHz modulated at 1 kHz to the test level AM depths given in the data sheet. Record the meter reading for each test level.
(Record Data)
- 5-27. Adjust the Signal Generator for 50% AM, \pm 3 dBm, and 118 MHz. Record the meter reading.
(Record Data)
- 5-28. Repeat paragraph 5-27 at 156 MHz. ()
- 5-29. Repeat paragraph 5-27 at 125 MHz and +7 dBm (corresponds to 50W transmitter at ANT jack).
(Record Data)
- 5-30. Repeat paragraph 5-27 at 125 MHz and -3 dBm (corresponds to a 5W transmitter at the ANT jack).
(Record Data)
- 5-31. Using the Modulation Meter adjust the Signal Generator for 100% AM modulation. Verify that the OVER MOD lamp is lighted. ()
- 5-32. With the Signal Generator adjusted for 50% AM, +3 dBm output, and 125 MHz, measure the dc and ac levels at J-21 DETECTOR OUT (back panel) using the DVM.
(Record Data)
- 5-33. Frequency Counter Accuracy. (3 ppm aging first year, 1 ppm afterwards, \pm 1 count).
- 5-34. Connect the Frequency Counter to Q203-collector on the Main Circuit Board and measure the frequency of the 10 MHz clock.
(Record Data)
- 5-35. Fault Sensing and Timing Circuitry.

5-36. Connect J-32, RECEIVER AUDIO OUT (back panel) to NAV-750's J-18, EXT MOD. Connect J2, NAV-750 REMOTE CHANNELING, and J6, NAV-750 ACCESSORY, to NAV-750 (see Fig 3-3). Connect NAV-750 RF output to J-16. ()

5-37. Control settings:

COMM-760

STANDBY/OPERATE STANDBY
 1V/10V. 10V
 NAV-750 EXT MOD ON (up)
 Meter Function Switch RCVR V
 AUDIO/RF. RF
 BYPASS. ON (All Three)
 NORMAL/PRINTER. NORMAL (Back Panel)
 ERROR LIMIT 2.0 kHz

NAV-750

1020Hz. Fully ccw, not in detent
 FREQUENCY 120.0015 MHz (use Δ F mode)
 AUTO/MANUAL MANUAL
 RF ATTENUATOR -6 dBm

- 5-38. Normal Mode Cycling. Adjust SET LIMIT (volts) 0.5V below the meter reading in MEASURE mode. Adjust R257, OFFSET (main circuit board), until Test Set's Power Meter reads 15W in the MEASURE MODE. ()
Adjust SET LIMIT (power) until the meter reads 10W in SET LIMIT mode. ()
These steps set up no-fault conditions for RCVR V and POWER fault circuits. Reset R257, OFFSET, (see paragraph 5-46) when completing Performance Check Procedures. ()
- 5-39. Set STBY/OPERATE to OPERATE and verify that the test set starts cycling between "receiver" and "transmitter keyed" modes at a rate determined by XMIT TIME control. ()
- 5-40. Verify that the cycling stops and the correct fault lamp lights when any of the following fault conditions are set into the controls:
- A) SET LIMIT (volts) is adjusted for a reading 1V Higher than in paragraph 5-38. ()
 - B) SET LIMIT (power) is adjusted for approximately 20W. ()
 - C) ERROR LIMIT is set to 1.0 kHz. ()

————— NOTE —————

After a fault condition is set into the controls, cycling stops, and the fault lamp is lighted. Continue cycling by removing the fault condition and pressing PUSH XMIT.

- 5-41. In sequence, set up fault condition in each of RCVR, PWR, and FREQ controls and verify that the fault can be bypassed using the correct BYPASS switch. (Three tests) ()
- 5-42. Set up no fault conditions into the controls. Set NAV-750's AUTO/MANUAL to AUTO. Verify that the test set cycles and that the NAV-750 Frequency Advance annunciator signals the channel advance of the NAV-750 output frequency. ()

Verify that the NAV-750 stops channeling and its
END lamp lights and the COMM-760 stops cycling as each of
117.950, 135.975, or 157.950 MHz is reached on the NAV-
750. ()

- 5-43. Printer Mode Cycling. (Optional) Connect the Digital
Printer to J-3, PRINTER (back panel). Set the controls
as in paragraph 5-36 and 5-37 except for the following:

COMM-760

NORMAL/PRINTER MODE. .PRINTER MODE (back panel)

ALL CHANNELS/FAULTS ONLY. ALL CHANNELS
(back panel)

NAV-750

AUTO/MANUAL. AUTO

- 5-44. Set STANDBY/OPERATE to OPERATE and verify that the Test
Set starts cycling (press PUSH XMIT if necessary). ()

Verify that the printer lists the channel frequency and
frequency error and either a "1" or a "0" appears in the
fault columns depending on whether or not a fault con-
dition has been set into the controls as in paragraph
5-40. ()

- 5-45. Set ALL CHANNELS/FAULTS ONLY to FAULTS ONLY. Verify
that the Test Set cycles but the printer is activated
only as long as a fault condition has been set into the
controls as in paragraph 5-40. ()

- 5-46. Reset R257, OFFSET (Main circuit board), for a reading
of zero on the POER METER with MEASURE/SET LIMIT (power)
in MEASURE. ()

Replace the Test Set's top cover.

SECTION VI

Calibration Procedure

- 6-1. Introduction.
- 6-2. The following instructions are used for calibration of the test set after a malfunction has been corrected or at periodic recertification dates. Allow a 30 minute warm-up period before starting these procedures. (See Table 5-1 for Recommended Equipment)

6-3. Calibration Procedure.

6-4. Main Circuit Board. (Refer to schematic Figure 9-1, Measurements Section Sheet 1)

A. Power Meter:

1. Adjust R257, Offset, until power meter reads zero.
2. Apply known amount of RF power to ANT jack. Adjust R1402, Power Cal (Front Panel Terminal Board), for correct reading of power meter. Verify that the PWR FAULT lamp lights when SET LIMIT is adjusted slightly greater than the above level and PUSH XMIT is depressed.

B. Tone Oscillator:

1. Place 1020/VAR to 1020. Connect an oscilloscope to the 2.5V P-P square waves at X221-9 (Fig 9-1). Adjust R266, Duty Cycle, for 50% duty cycle.
2. Turn meter function to TONE V, turn TONE LEVEL full cw and connect a distortion analyzer to J22-ring, MICROPHONE. Adjust R267 and 268, Distortion, and R266, Duty Cycle, for minimum distortion (1% maximum).
3. Verify: Sine wave at P11-16 is approximately 3.5V rms. ()
4. Verify: Sine wave at P11-4 (or at J22-ring) is approximately 1.8V rms with TONE LEVEL fully cw. Distortion is 1% maximum. ()
5. Place RF/AUDIO to AUDIO. Adjust R1406, 1020Hz (Front Panel Terminal Board), for 1.020 kHz \pm 2Hz display.
6. Place 1020/VAR to VAR, HI/LOW to HI, and TONE FREQ fully cw. Adjust R1411 HI Frequency (Front Panel Terminal Board) for 13.050 kHz \pm 50Hz.
7. Place HI/LOW to LOW and TONE FREQ fully ccw. Adjust R1409, LO FREQUENCY (Front Panel Terminal Board), for 0.140 kHz \pm 10Hz. Repeat 6 and 7 if necessary.

C. Notch Filter: (Refer to schematic Figure 9-2, Measurements Section Sheet 2.)

1. Place meter function switch to TONE V. Adjust R296, Notch Q, mid-range. Adjust TONE LEVEL fully cw and TONE FREQ for 1020Hz.
2. Connect oscilloscope to X227-7 (sync at X225-1). Adjust R293, F0, and R295, Q, for minimum 1020Hz signal at X227-7.
3. Adjust TONE FREQ for approximately 700Hz. Measure ac signal at X225-1 (reference level). Adjust R296, Notch Q, until X227-7 reduces to approximately one half the above reference value at 990 and 1060 (6dB bandwidth of 70Hz \pm 10Hz).

D. Divider (S+N/N Circuit):

1. Place Meter Function switch to TONE V and adjust TONE FREQ for approximately 700Hz and TONE LEVEL fully CW.
2. Place S201-1 and S201-4 to OFF. Ground TP202.
3. Connect oscilloscope to TP201 (sync at X225-1). Adjust R2009, P-3, for minimum ac voltage. Adjust R2008 P-I, for zero volts dc.
4. Remove ground on TP202. Place S201-2 to ON, S201-3 to OFF. Adjust R2010, P-2, for minimum ac voltage at TP201. Return S201-2 to OFF and S201-3 to ON.
5. Return S201-1 to ON, S201-2 to OFF, S201-3 to ON, and S201-4 to ON. Repeat 2 through 4.
6. Jumper J6-1 (NAV-750 EXT MODULATION) to J1-18 (RCVR AUDIO INPUT). Place Meter Function to S+N/N and NAV-750 EXT MOD to ON (up). Measure the negative dc level at X226A-1 (reference level) with a DVM. Place 1020/VAR to VAR and HI/LOW to LOW. Adjust TONE FREQ (to approximately 1060Hz) until the positive dc level at X228A-1 is 0.48 times the magnitude of the above reference level. Adjust R2021, S+N/N Cal, until the meter reads 6dB.

7. Adjust TONE FREQ until meter reads 6dB. Adjust R2016, 6dB Limit Cal, until RCVR FAULT lamp just lights. Remove jumper.
8. AGC Amplifier Range. Place Meter Function switch to RCVR V. Connect an audio oscillator to J-32, REC AUDIO OUT. Vary the oscillator's level between 0.1 and 10V rms and verify that the AGC amplifier output at X225-1 is within the range of 3.31 to 4.05V rms. ()

E. Voltmeter:

1. Connect audio oscillator to J-32, REC AUDIO OUT. Place Meter Function to RCVR V and 1V/10V to 10V. Adjust oscillator for 5.00V rms at 1 kHz.
2. Adjust R1403, 10V CAL, (Front Panel Terminal Board), for exactly half scale reading (5.0V).
3. Adjust oscillator for 0.50V rms. Place 1V/10V to 1V, and verify that meter reads 0.485 to 0.515V rms. ()

F. Peak Detector (% Modulation Circuit):

1. Apply a +3 dBm, approximately 120 MHz RF signal to J-16, input of AGC Detector module. Set RF signal modulation to 80% AM at 1 kHz.
2. Place Meter Function switch to % MOD. Adjust R2025, 100% Mod Cal, for meter reading of 80 \pm .5%.
3. Adjust modulation of RF source for just below 100% (approximately 98%). Adjust R2039. Over-mod Limit, until OVERMOD lamp just lights.

G. 10 MHz Clock: (Refer to schematic Figure 9-3, Clock Circuit.)

1. Connect the frequency counter to the collector of Q203, clock buffer. Adjust C203 for 10 MHz \pm 2Hz (\pm .00002%) counter reading.
2. An alternate method would be to zero beat this clock with WWV (10 MHz) and adjust C203 for a beat of less than 2Hz.

6-5 Counter Gating Board. (Refer to schematic Figure 9-5,
Error Frequency Counter.)

A. Blanking Monostable (X701):

1. Place RF/AUDIO to RF. Connect oscilloscope to X707-11 and adjust R707 for a 2.5ms "0" level pulse

SECTION VII

Semiconductor and IC Guide

- 7-1. Introduction.
- 7-2. The COMM-760 Test Set utilizes a wide range of semiconductors and IC devices to accomplish its purpose. Although all solid-state components have been in general use for many years now, it is still manufacturer's experience that improper repair of printed circuit boards and use of test devices not suited to transistors cause far too many failures that can be easily avoided. The intent of this section is to familiarize the repair technician with approved methods of living with the modern technology.
- 7-3. This section is divided into two general areas - the repair of solid-state equipment in a manner that will prolong the equipment life, and a familiarization with the various IC's used and how to determine their proper operation.
- 7-4. Semiconductor Test Equipment. Damage to semiconductors by test equipment is usually the result of accidentally applying too much current or voltage to the elements. Common causes of damage from test equipment are discussed in the following paragraph.
- 7-5. Transformerless Power Supplies. Test equipment with transformerless power supplies is one source of high current. However, this type of test equipment can be used by employing an isolation transformer in the ac power line.
- 7-6. Line Filter. It is still possible to damage semiconductors from line current, even though the test equipment has a power transformer in the power supply, if the test equipment is provided with a line filter. This filter may function as a voltage divider and apply half voltage to the semiconductor. To eliminate this condition, connect a ground wire from the chassis of the test equipment to the chassis of the equipment under test before making any other connections.
- 7-7. Low-Sensitivity Multimeters. Another cause of semiconductor damage is a multimeter that requires excessive current to provide adequate indications. Multimeters with sensitivities of less than 20,000 -ohms-per-volt should not be used on semiconductors. A multimeter with low sensitivity will draw too much current through many types of small semiconductors

causing damage. When in doubt as to the amount of current supplied by a multimeter, check the multimeter circuits on all scales with an external, low-resistance multimeter connected in series with the multimeter leads. If more than one milliampere is drawn on any range, this range cannot be safely used on small semiconductors.

- 7-8. **Power Supply.** When using a battery-type power supply, always use fresh batteries of the proper value. Make certain that the polarity of the power supply is correct for the equipment under test. Do not use power supplies having poor voltage regulation.

Due to the wide utilization of semiconductors in this electronic equipment, somewhat different techniques are necessary in maintenance procedures. In solid-state circuits, the impedances and resistances encountered are of much lower values than those encountered in vacuum-tube circuits. Therefore, a few ohms discrepancy can greatly affect the performance of the equipment. Also, coupling and filter capacitors are of larger values and usually are of the tantalum type. Hence, when measuring values of capacitors, an instrument accurate in the high ranges must be employed. Capacitor polarity must be observed when measuring resistance. Usually more accurate measurements can be obtained if the semiconductors are removed or disconnected from the circuit.

7-9. Replacing Semiconductors.

- 7-10. (1) Transistors. Never remove or replace a transistor with the supply voltage turned on. Transients thus produced may damage the transistor or other components remaining in the circuit. If a transistor is to be evaluated in an external test circuit, be sure that no more voltage is applied than that applied during actual use.

- 7-11. (a) Use only a low heat soldering iron when installing or removing soldered in parts.

- 7-12. (b) When installing or removing a soldered in semiconductor grasp the lead to which heat is applied between the solder joint and the semiconductor with long nose pliers. This will dissipate some of the heat that would otherwise conduct into the semiconductor from the soldering iron. Make certain that all wires soldered to semiconductor terminals have first been properly tinned so that the necessary connections can be made quickly. Excessive heat will permanently damage a semiconductor.

- 7-13. (c) In some cases, power transistors are mounted with heatsinks that are designed to dissipate heat away from them. In some power circuits, the transistor must also be insulated from ground. Often, this insulating is accomplished by means of insulating washers made of mica. When replacing transistors mounted in this manner, be sure that the insulating washers are replaced in proper order. After the transistor is mounted, and before making any connections check from the case of the transistor to ground with a multimeter to see that the insulation is effective.
- 7-14. (2) Integrated Circuits. If an IC is known to be defective, the best way to remove it is to cut off each of its pins, remove the case, and then unsolder the remaining pins from the integrated circuit card one by one. This is preferable over removing the IC intact because attempts to remove the IC intact may result in damage to the card. Note the marking identification of the IC before removal, and replace the new one with the same orientation as the one removed.

7-15. Following is a list of the IC's, their circuit functions, and board locations.

<u>SN7400</u>	Counter Gating Board
(Quad 2-input NAND gate)	Timer Section -
	Main Circuit Board
	Counter Logic Board
	RF/Audio Frequency
	Counter Board
	Frequency Error Counter Board
<u>SN7402</u>	Frequency Error Counter Board
(Quad 2-input NOR GATE)	Counter Gating Board
<u>SN7420</u>	Timer Section -
(Dual 4-input NAND gate)	Main Circuit Board
<u>SN7430</u>	Frequency Error Counter Board
(Single 8-input NAND gate)	

<u>SN7473</u> (Dual J-K Flip-Flop)	Clock Circuit-Main Circuit Board Timer Section-Main Circuit Board RF/Audio Frequency Counter Board Frequency Error Counter Board Counter Logic Board Counter Gating Board.
<u>SN7475</u> (Quadruple Bistable latch)	Frequency Error Counter Board Counter Logic Board
<u>SN7490</u> (Divide by 2,5 or 10)	RF/Audio Frequency Counter Board Clock Circuit-Main Circuit Board Counter Logic Board
<u>SN74121N</u> (Monostable Multi-vibrator)	Frequency Error Counter Board Timer Section-Main Circuit Board Counter Gating Board
<u>SN74123</u> (Dual Retriggerable Monostable Multi-vibrators)	Timer Section-Main Circuit Board Frequency Error Counter Board Counter Gating Board
<u>SN74190</u> (Synchronous Up/Down Decade Counters)	Frequency Error Counter Board
<u>SN72558P, MC1458</u> (Dual-Operational Amplifier)	Measurement Section-Main Circuit Board AGC/Detector Board
<u>SN72741L</u> (Compensated operational amplifier)	Clock Circuit-Main Circuit Board Measurement Section-Main Circuit Board
<u>SN74S00</u> (Schottky Quadruple 2-input positive NAND Gate)	RF/Audio Frequency Counter Board

<u>SN74S112</u> (Schottky Dual J-K Edge triggered Flip- Flop)	RF/Audio Frequency Counter Board
<u>DD-700</u>	Frequency Error Counter Board Counter Logic Board
<u>MC1494L</u> (Linear Four Quad- rant Multiplier	Measurement Section-Main Circuit Board
<u>MC1709CG</u> (High Performance operational-amp- lifier	Measurement Section-Main Circuit Board
<u>MC12013</u> (Two Modulus Pre- scaler)	Prescaler ÷ 10 Board
<u>LM307H</u> (Compensated and protected operational amplifier)	AGC/Detector Board
<u>LM309K</u> (5V Voltage Reg- ulator)	Power Supply
<u>LM320K-12</u> (-12V Voltage Reg- ulator)	Power Supply
<u>LM340K-12</u> (+12V Voltage Reg- ulator)	Power Supply
<u>μA706BP</u>	Measurement Section-Main Circuit Board

7-16. General Operation of Digital IC's.

7-17. All digital "elements" (gate, counters, comparators, etc.), operates on a two level basis. One level is termed "logic zero" or L0 and is any voltage less than 0.8V. (Normally logic zero is 0.2V). The other level is termed

"logic one" or HI and is any voltage greater than 2.0V. (Normally logic one is +3.2V). In positive logic circuits the Logic One is always the more positive voltage level. Negative logic - not used in the COMM-760 - has Logic One the more negative voltage level.

7-18. In paragraph 7-17 is stated that normal logic levels are 0.2V (0) and 3.2V (1). In the prescaler three flip-flops ÷ 2 IC's are used which operate below 0 volts. Logic 0 is 3.3V and logic 1 is 4.1V. Notice logic 1 is still more positive.

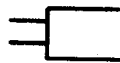
7-19. SN7400 Quad 2 input NAND Gate. This "quad" gate pack is very versatile in design. The SN7400 is normally shown as



, which indicates it requires two logic one state at the inputs to cause a logic zero state to occur at the output. The small (zero)



shown at the output tells the output state when the input state is satisfied - in this case two logic one levels



(no zeros are indicated). Notice that if either input level goes down to a logic zero the output must go up to a logic one. The SN7400 may be used as a NOR gate in this way as is shown



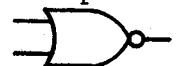
Read the symbol as "OR function" requiring a logic zero on either input to cause a one level to appear at the output. Thus the SN7400 is both:



OR



7-20. SN7402 Quad 2 input NOR Gate. This is the compliment of the SN7400 and thus is normally shown as



Read this symbol to say "it requires a logic one on either input to cause a logic zero output state". This implies that both inputs are used in the zero state and raised to one state during operation. This also means that the output will be up - logic one - only if both inputs are logic zeros. Therefore this gate can also be used as a NAND gate requiring two zeros at the input to cause a one at the output. It is drawn as:

The SN7402 is both:



OR



- 7-21. The SN7420 has two packs of four inputs each, and are similar to the SN7400. They may be used as:



- 7-22. SN7430 Single 8-input NAND Gate. The 7430 is an 8-input NAND gate which operates similar to the SN7400. All 8 inputs must be high for the output to go low. If any input is low the output will go high.
- 7-23. SN7443BCD to Decimal Decoder. The 7442 accept 1,2,4,8 BCD data at the inputs and for the corresponding BCD number 0-9 causes one of ten outputs to go low. Therefore, four lines of BCD data are decoded into ten lines of data.
- 7-24. The SN7473 J-K Flip-Flop. Logic element is the basic storage and control element of the COMM-760 logic. It uses one "clock" input which controls the device in conjunction with two other inputs called "J" and "K" inputs. The clock pulse required is a transistion from a "one" to a "zero" state. If "J" is up (logic one) a clock pulse will "set" the flip-flop and cause "Q" output to go to a logic "one" and " \bar{Q} " output to go to a logic "zero". (This is the definition of "set".) If K is up the clock pulse will "reset" the flip-flop and cause "Q" to go down and " \bar{Q} " to go up. If both J and K are up the input clock frequency will be divided by two. If only one input is up (J or K) the first clock pulse will either set or reset the device and succeeding clock pulses will have no effect. A direct reset input is provided which when raised to the logic one level will force the SN7473 to reset. As long as the direct reset line is up all clock pulses have no effect - the device will stay reset.
- 7-25. SN7475. The 7475 is a quad latch. It consists of four identical but independent stages. Data present at the inputs is transferred to the outputs as long as the clock input is high. When the clock input goes low the data that was present at the input at that instant will be stored at the data output.
- 7-26. The SN7490 Divider. The SN7490 is an element capable of dividing by 2,5, or 10 in binary format. It requires downward clock transitions to change states and count.

Therefore a small logic zero is shown at each clock input. The device uses one flip-flop at the input independent of all others and is used as a divide-by-2 function. Three other flip-flops are internally connected to divide-by-5. When externally connected in series a divide-by-10 function is formed. A logic one on any output indicates that output is to be added to the sum stored at that instant in the SN7490.

- 7-27. The SN7490 may be reset to either a "zero" count or "nine" count by the application of two logic "one" levels to either the R0 or R9 inputs. Both R0 or R9 inputs must be up (added) to achieve reset. Also, while either R0 or R9 inputs are up all input clock pulses are thrown away and have not effect.
- 7-28. SN74121N Monostable Multivibrator. The SN74121N is a oneshot element with gated inputs. External R and C values must be added to form pulse widths from 40ns to 40 seconds. Three inputs provide selective gating. If B is held at a logic "one" state, a logic "zero" on either A1 or A2 will trigger an output pulse; or if either A1 or A2 is held low an upclock on B will trigger a pulse. The device is used in the COMM-760 to widen an extremely narrow reset pulse to useable proportions.
- 7-29. SN74123. Dual One-Shot operates the same as the 74121 except there are two in one package.
- 7-30. SN74190 Synchronous Up/Down Decade Counter. One line controls whether the device counts up or counts down. All output stages change state at the same time. Typical clock frequencies are in excess of 20 MHz.
- 7-31. 72558P, 5558, or MC1458. These dual operational amplifiers contain two operational amplifiers with each electrically similar to the SN72741. All internal frequency compensation keeps external components to a minimum. They are used wherever a general purpose amplifier is required. These three are interchangeable in operation. (See 7-32)
- 7-32. SN72741L Single Compensated Op Amp. The SN72741L is a single operational amplifier with internal frequency compensation. It is used when a high performance op amp is required. (See 7-31)
- 7-33. SN74S00 Schottky Quadruple Two Input Positive NAND Gate. Identical to SN7400 discribed in 7-19 except it is capable of speeds of 80 MHz whereas the SN7400 is capable of 20 MHz maximum.

- 7-34. SN74S112 Schottky Dual J-K Edge Triggered Flip-Flop. Like the 74S00 in 7-33, the 74S112 is capable of speeds of 80 MHz. (Similar to SN7473 in 7-24)
- 7-35. The DD-700 BCD to 7-Bar HV Display Decoder. The DD-70 is designed to operate high voltage gas-discharge readouts such as the Sperry used in the COMM-760. It can safely handle output voltage as high as 180-200 volts. The DD-700 requires a 5V power supply for its own operation. Its current regulates the output to maintain even display brightness.
- 7-36. MC1494L Linear Four Quadrant Multiplier. The MC1494L output voltage is a linear product of two input voltages. The MC1494L may be used to multiply, divide, square root etc., and is used in the COMM-760 as a divider. With external potentiometers, this device provides complete adjustability of scale factor, as well as input and output offsets. Voltage regulator and level-shift circuitry are internal.
- 7-37. MC1709CG High Performance Operational Amp. The MC1709CG is a higher speed high performance operational amp. It requires external frequency compensation otherwise operates similar to the SN72741L. (See 7-39 and 7-42)
- 7-38. MC12013 Two Modulus Prescaler. This device is designed to operate at a 600 MHz Toggle Frequency and will divide by 10 and 11. The MC12013 has a buffered clock input, an ECL to TTL translator, TTL and ECL Enable inputs, and provides a VBB Reference Voltage.
- 7-39. LM307H Compensated and Protected Operational Amplifier. The LM307H is a single, two input general purpose operational amplifier with frequency compensation and overload protection on the input and output currents. Input currents are a factor of ten lower than most other operational amplifiers. The LM307 is a direct plug in replacement for MC1709CG or SN72741L.
- 7-40. LM309K, LM320K-12, and LM340K-12 Voltage Regulators. These are one piece integrated positive voltage regulators, complete in themselves. They require no external components except for transformers, rectifiers and filter capacitors. Each regulator is set for a specific voltage.

7-41. μA706BP Linear Audio Amplifier. This device is designed to deliver 5.5W continuous output when provided with adequate heat sinking. Special features are: self-centering bias; direct coupling to input; low quiescent current; high input impedance; low distortion; high peak output current; and high immunity to short-circuited output (Max Junction Temperature 150 degrees centigrade)

7-42. through 7-55. Intentionally omitted.

7-56. Operational Checking of IC's.

- 7-57. The usual method of verifying that an IC of any function is working properly is to observe it in action in the circuit. If the IC is of TTL (Transistor-transistor logic), which most all the IC's are in the COMM-760, the input levels must go below 0.4V and above 2.4V for well defined logic "zero" and "one" levels. Output levels usually will go from 0.2 or 0.3V to 3.2V. Gate packs must perform per their logic functions which can be verified with an oscilloscope. Counter IC's should divide the input clock frequency by 2, 4, 8 and 10 observing the 2^0 (1 or A), 2^1 (2 or B), 2^2 (4 or C) and 2^3 (8 or D) output.
- 7-58. IC's of any type are designed to sense changing voltage levels at their inputs. This causes them to be particularly sensitive to both power buss variations and noise picked up in various ways on the toggle or clock lines. When IC failure is suspected always observe the A+ leads near the IC's. Be aware of transients from external sources varying enough in amplitude to fall below 1.5V. Sometimes a faulty IC will introduce transients onto clock lines to other IC's making them appear faulty also.

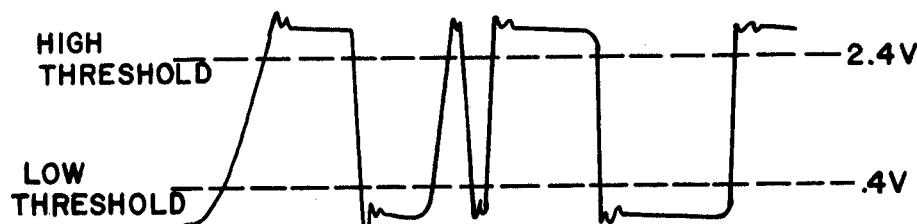


Fig 7-1

Figure 7-1. TTL Signal. In digital electronics, the relative value of signal voltage with respect to the threshold voltages determines the operation of the circuit. A signal above the high threshold is in the high state and whether it is 2.8V or 3.0V is irrelevant to the logical operation of the circuit.

- 7-59. Figure 7-1 shows a typical TTL (Transistor-transistor logic) signal. This might as well be any analog signal when viewed on an oscilloscope. The oscilloscope displays absolute voltage with respect to time, but in digital electronics absolute values are unimportant. A digital

signal exists in one of two or three states--high, low, and undefined or in-between level--each determined by a threshold voltage. It is the relative value of the signal voltage with respect to these thresholds that determines the state of the digital signal and this digital state determines the operation of the IC, not absolute levels. In Figure 7-1 if the signal is greater than 2.4 volts, it is a high state and it is unimportant whether the level is 2.8 or 3.0 volts. Similarly for a low state the voltage must be below .4 volts. It is not important what the absolute level is as long as it is below this threshold. Thus when using an oscilloscope, the troubleshooter must over and over again determine if the signal meets the threshold requirements for the desired digital state.

- 7-60. Within a digital logic family, such as TTL, the timing characteristics of each component are well defined. Each gate in the TTL logic family displays a characteristic propagation delay time, rise time, and fall time. The effects of these timing parameters on circuit operation are taken into account by the designer. Once a design has been developed beyond breadboard or prototype stage and is in production problems due to design have hopefully been corrected. An important characteristic of digital IC's is that when they fail, they fail catastrophically. This means that timing parameters rarely degrade or become marginal. Thus observing on an oscilloscope and making repeated decisions on the validity of timing parameters is time consuming. Once problems due to design are corrected, the fact that pulse activity exists is usually enough indication of proper IC operation without further observation of pulse width, repetition rate, rise time or fall time.

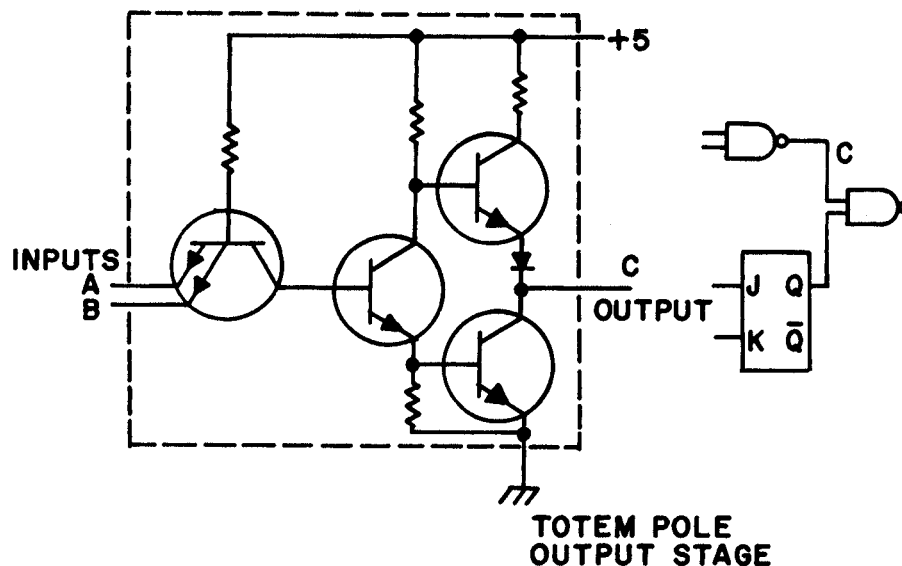


Fig. 7-2

Figure 7-2. When stimulating a node in circuit, such as C above, it is necessary to override the low impedance totem pole output stage driving that node. When the output is in the low state, it is a saturated transistor to ground. Presently used signal sources are not powerful enough to override this low state.

- 7-61. Figure 7-2 shows a problem created by the TTL logic family. The output stage of a TTL device is a transistor totem pole. In either the high or low state, it is a low impedance. In the low state it is a saturated transistor to ground. It thus appears as 5--10 ohms to ground. This presents a problem to in-circuit stimulation. A signal source used to inject a pulse at a node which is driven by a TTL output must have sufficient power to override the low impedance output.

FAILURE MODES OF DIGITAL IC's

- 7-62. In order to troubleshoot efficiently, it is important to understand the type of failures found in digital circuits. These can be categorized into two main classes --those caused by a failure internal to an IC and those caused by a failure in the circuit external to the IC.
- 7-63. There are four types of failures that can occur internally to an IC. These are (1) an open bond on either an input or output, (2) a short between an input or output and Vcc or ground, (3) a short between two pins (neither of which are Vcc or ground), and (4) a failure in the internal circuitry (often called the steering circuitry) of the IC.
- 7-64. In addition to these four failures internal to an IC, there are four failures that can occur in the circuit external to the IC. These are (1) a short between a node and Vcc or ground, (2) a short between two nodes (neither of which are Vcc or ground), (3) an open signal path, and (4) a failure of an analog component.

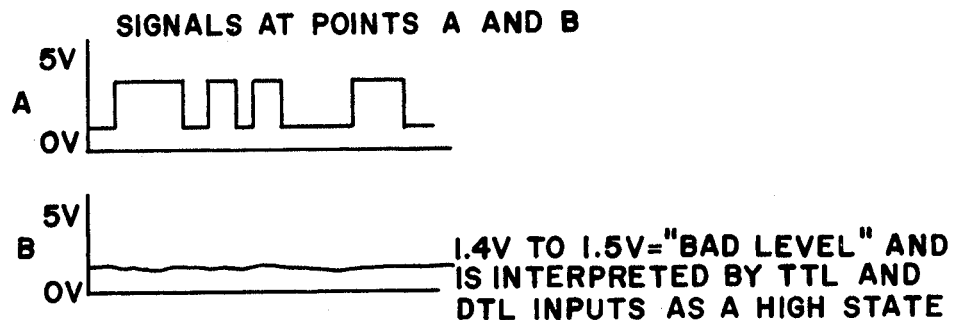
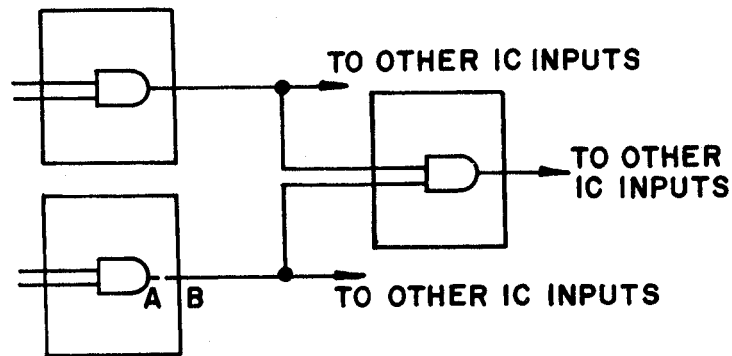


Fig. 7-3

Figure 7-3. The Effect of an Open Output Bond Upon Circuit Operation. An open output bond allows all inputs driven by that output to float to a "bad level". This level is usually interpreted as a logic high state by the inputs. Thus the inputs driven by an open output bond will respond as though a static logic high signal was applied.

- 7-65. Before discussing how to detect each of these failures we will discuss the effect each has upon circuit operation. The first failure internal to the IC mentioned was an open bond on either an input or output. This failure has a different effect depending upon whether it is an open output bond or an open input bond. In the case of an open output bond (Figure 7-3), the inputs driven by that output are left to float. In TTL and DTL circuits a floating input rises to approximately 1.4 to 1.5 volts and usually has the same effect on circuit operation as

a high logic level. Thus an open output bond will cause all inputs driven by that output to float to a bad level since 1.5 volts is less than the high threshold level of 2.4 volts and greater than the low threshold level of .4 volts. In TTL and DTL, a floating input is interpreted as a high level. Thus the effect will be that these inputs will respond to this bad level as though it were a static high signal.

- 7-66. In the case of an open input bond (Figure 7-4), we find that the open circuit blocks the signals driving the input from entering the IC chip. The input on the chip is thus allowed to float and will respond as though it were a static high signal. It is important to realize that since the open occurs on the input inside the IC, the digital signal driving this input will be unaffected by the open and will be detectable when looking at the input pin (such as at Point A in Figure 7-4). The effect will be to block this signal inside the IC and the resulting IC operation will be as though the input were a static high.

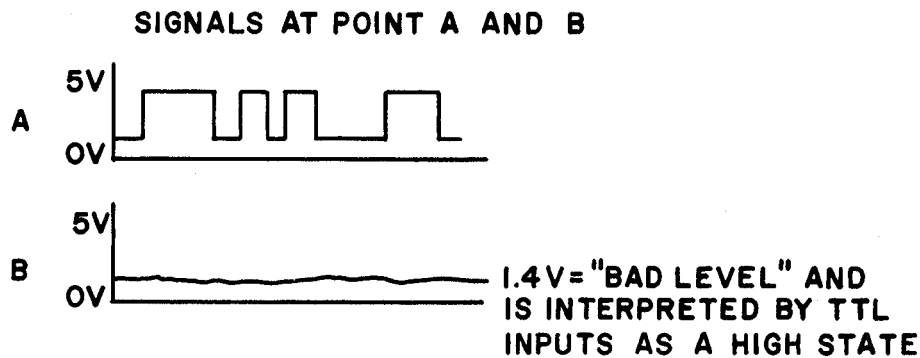
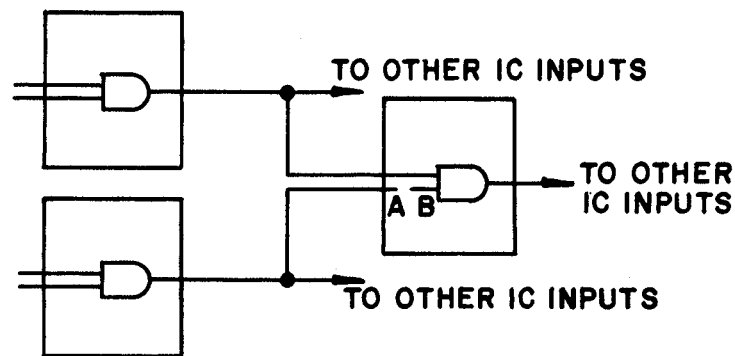


Fig. 7-4

Figure 7-4. The Effect of an Open Input Bond Upon Circuit Operation. An open bond on an input has the effect of blocking the input signal from reaching the chip and allows the input of the chip to float to a "bad level". Thus even though the signal can be viewed at an external point such as Point A, the input of the chip responds to the "bad level" as though it were a static high level.

- 7-67. A short between an input or output and Vcc or ground has the effect of holding all signal lines connected to that input or output either high (in the case of a short to Vcc) or low (if shorted to ground)(Figure 7-5). In many cases, this will cause expected signal activity at points beyond the short to disappear and thus this type of failure is catastrophic in terms of circuit operation.

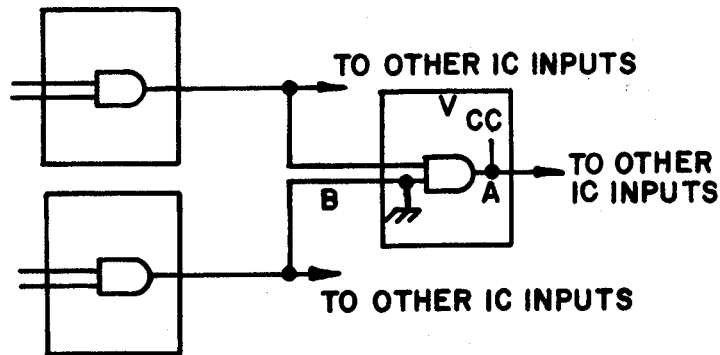
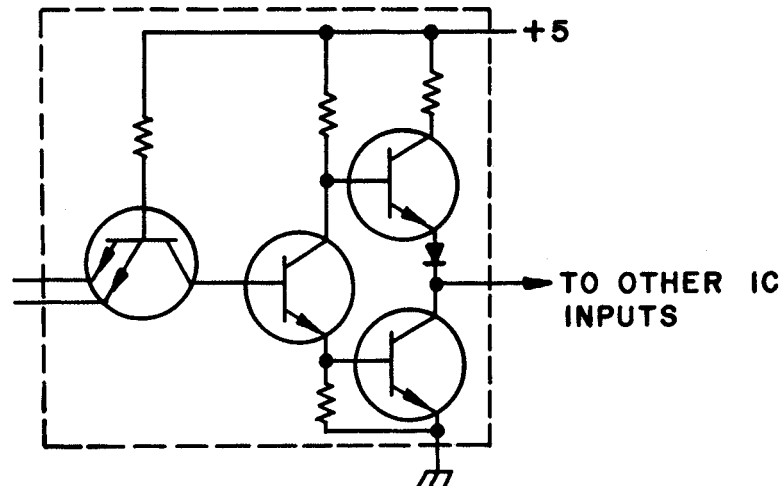


Fig 7-5

Figure 7-5. The Effect of a Short Between an Input or Output and V_{CC} or Gnd. All signal lines connected to Point A are held in the high state. All signal lines connected to Point B are held in the low state.

- 7-68. A short between two pins is not as straightforward to analyze as the short to V_{CC} or ground. When two pins are shorted the outputs driving those pins oppose each other when one attempts to pull the pins high while the other attempts to pull them low (Figure 7-8). In this situation the output attempting to go high will supply current through the upper saturated transistor of its totem pole output stage while the output attempting to go low will sink this current through the saturated lower transistor of its totem pole output stage. The net effect is that the short will be pulled to a low state by the saturated transistor to ground. Whenever both outputs attempt to go high simultaneously or to go low simultaneously, the shorted pins will respond properly. But whenever one output attempts to go low the short will be constrained to be low.

- 7-69. The fourth failure internal to an IC is a failure of the internal (steering circuitry of the IC - figure 7-6). This has the effect of permanently turning on either the upper transistor of the output totem pole thus locking the output in the high state or turning on the lower transistor on the totem pole thus locking the output in the low state. Thus this failure blocks the signal flow and has a catastrophic effect upon circuit operation.



STEERING CIRCUITRY

Fig 7-6

Figure 7-6. The Effect of a Failure of the Internal Circuitry of the IC Upon Circuit Operation. A failure of the steering circuitry of an IC will either cause the output to be in a static high state or a static low state.

- 7-70. A short between a node and Vcc or ground external to the IC is indistinguishable from a short internal to the IC. Both will cause the signal lines connected to the node to be either always high (for shorts to Vcc) or always low (for shorts to ground). When this type of failure is encountered only a very close physical examination of the circuit will reveal if the failure is external to the IC.

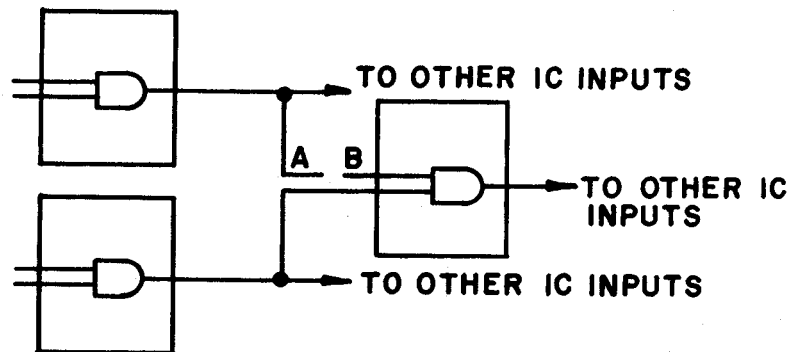


Fig 7-7

Figure 7-7. The Effect of an Open in the Circuit External to an IC. All inputs attached to the node at Point A will be driven properly. All inputs to the right of the open (Point B) will be left to float to a "bad level" and will therefore look like a static high state.

- 7-71. An open signal path in the circuit has a similar effect as an open output bond driving the node (Figure 7-7). All inputs to the right of the open will be allowed to float to a bad level and will thus appear as a static high level in circuit operation. Those inputs to the left of the open will be unaffected by the open and will thus respond as expected.

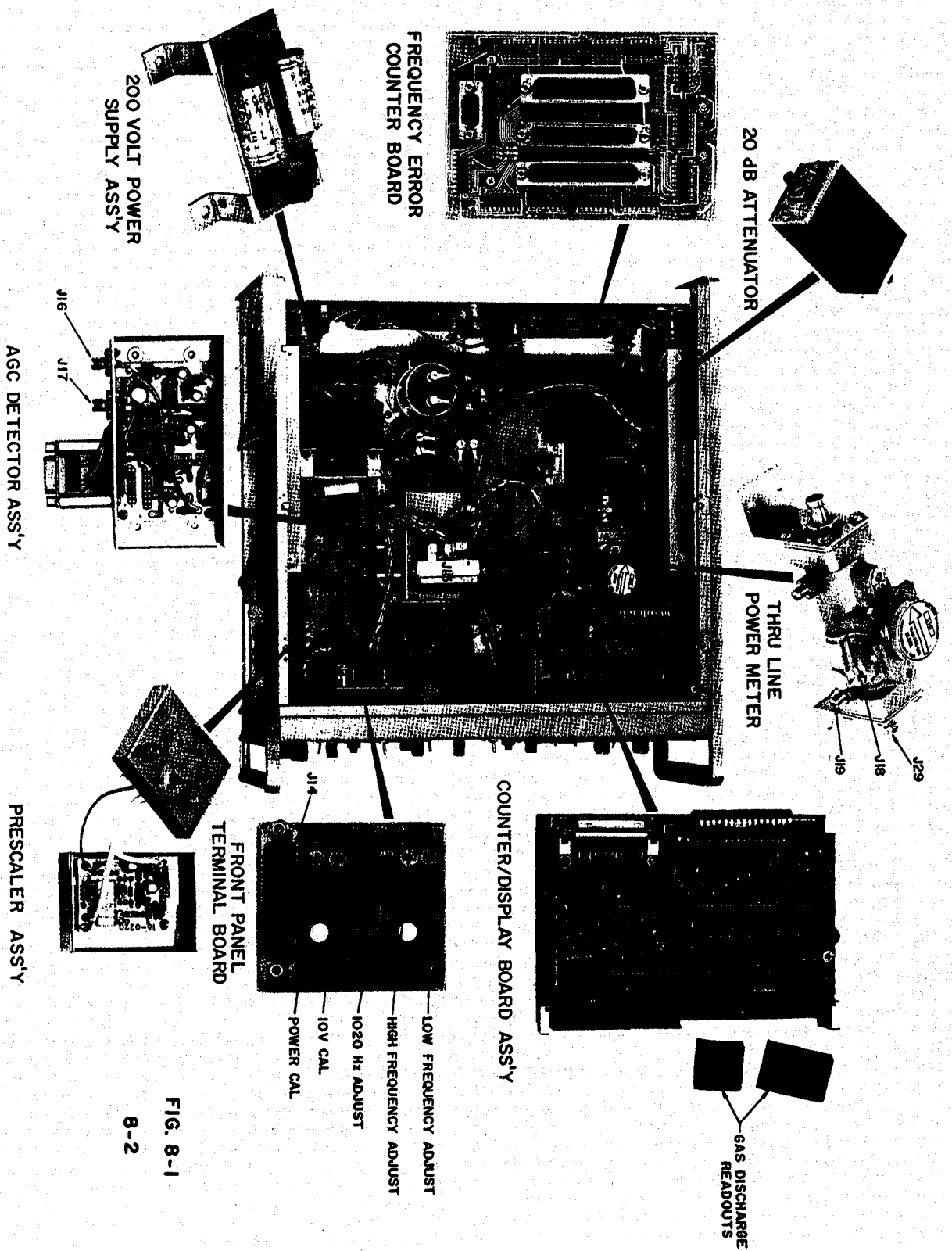
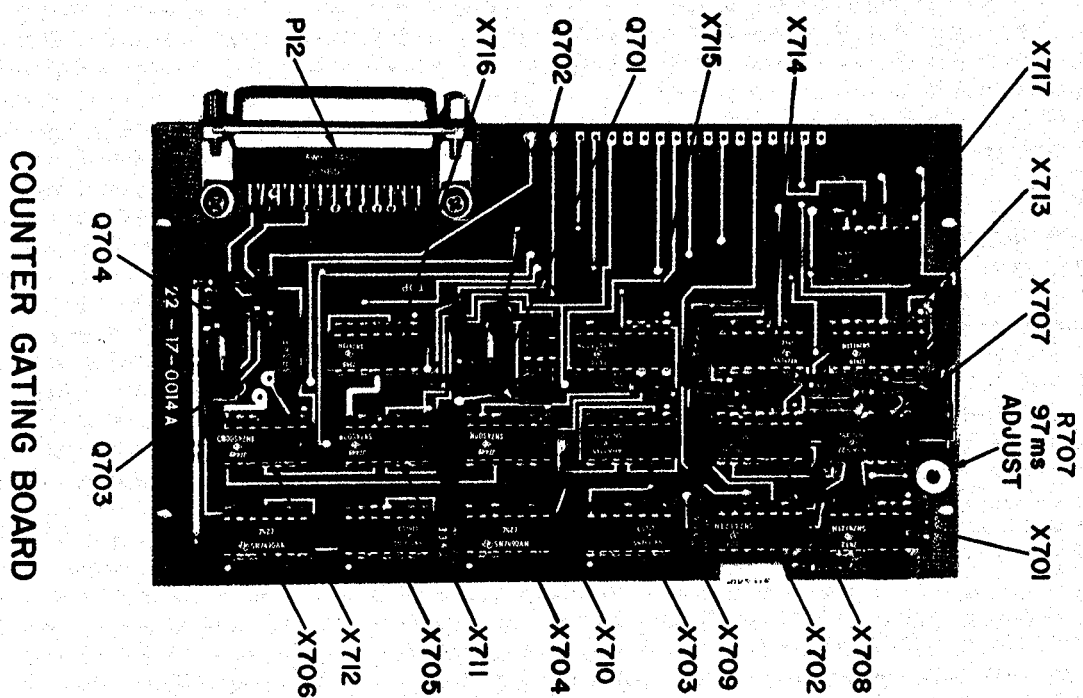
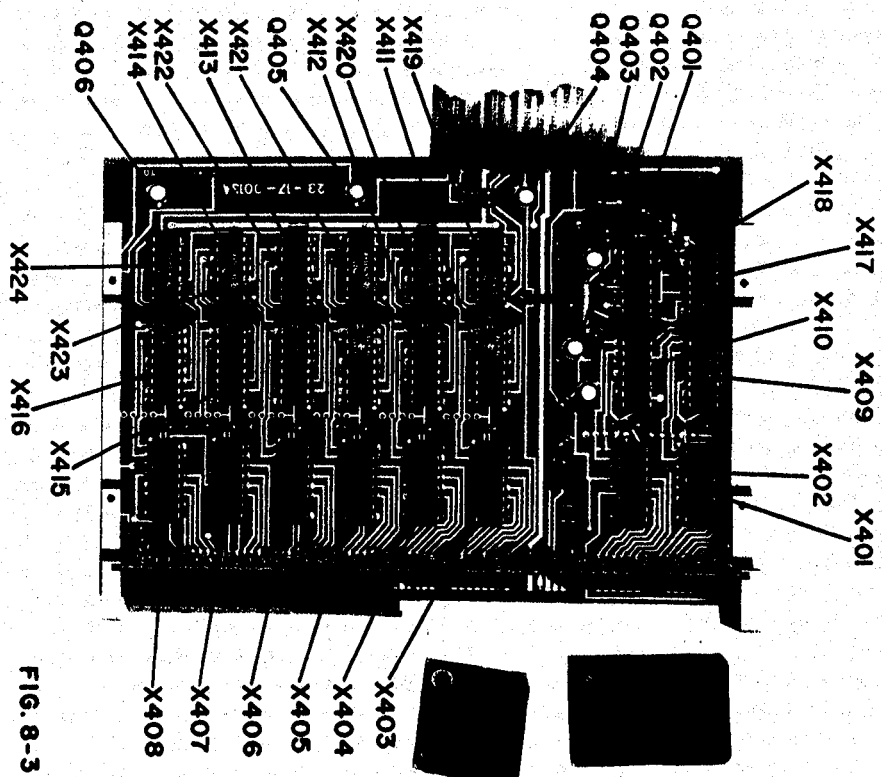


FIG. 8-1
8-2



COUNTER GATING BOARD



COUNTER LOGIC BOARD

PRESALER ASSEMBLY

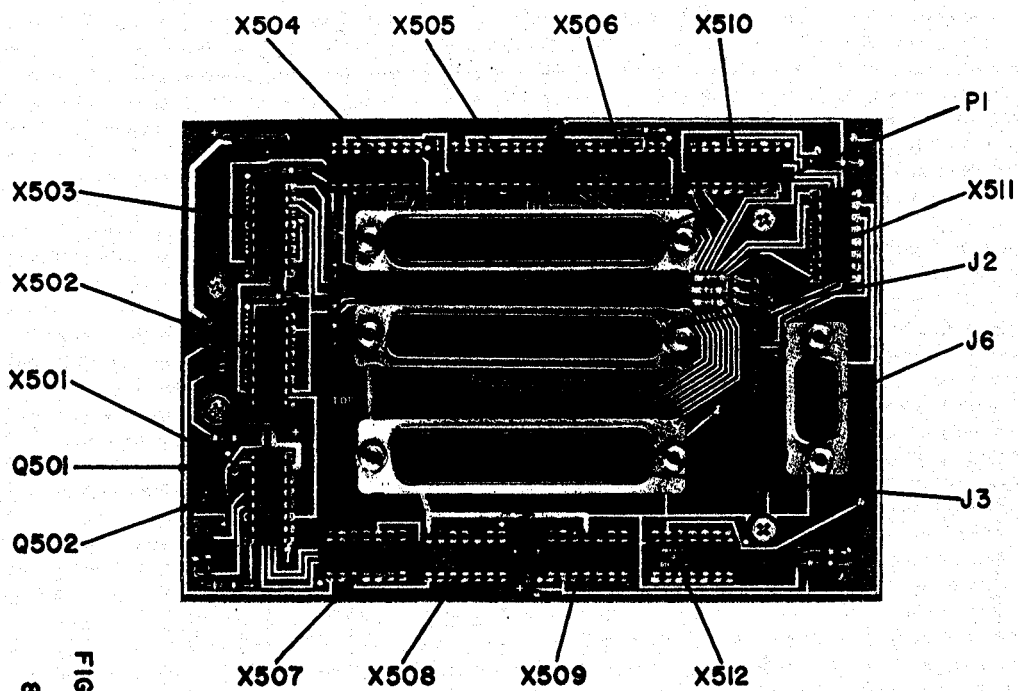
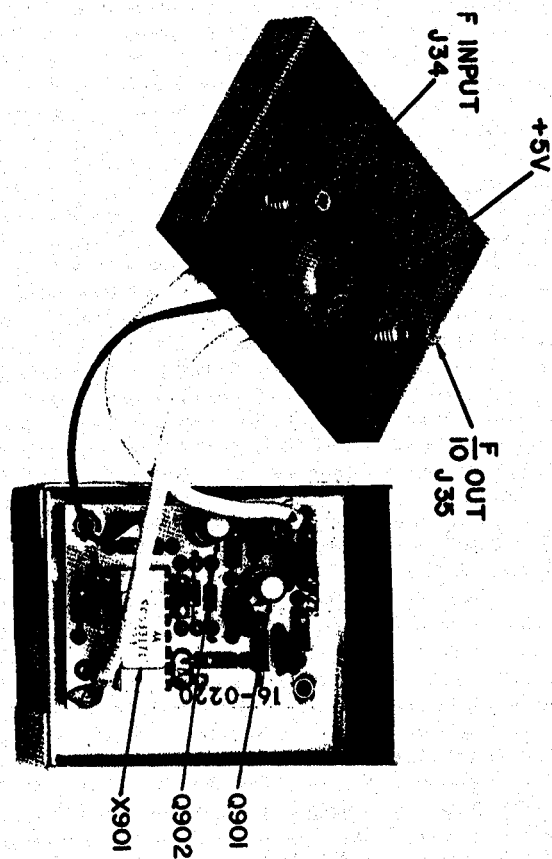


FIG. 8-4
8-5

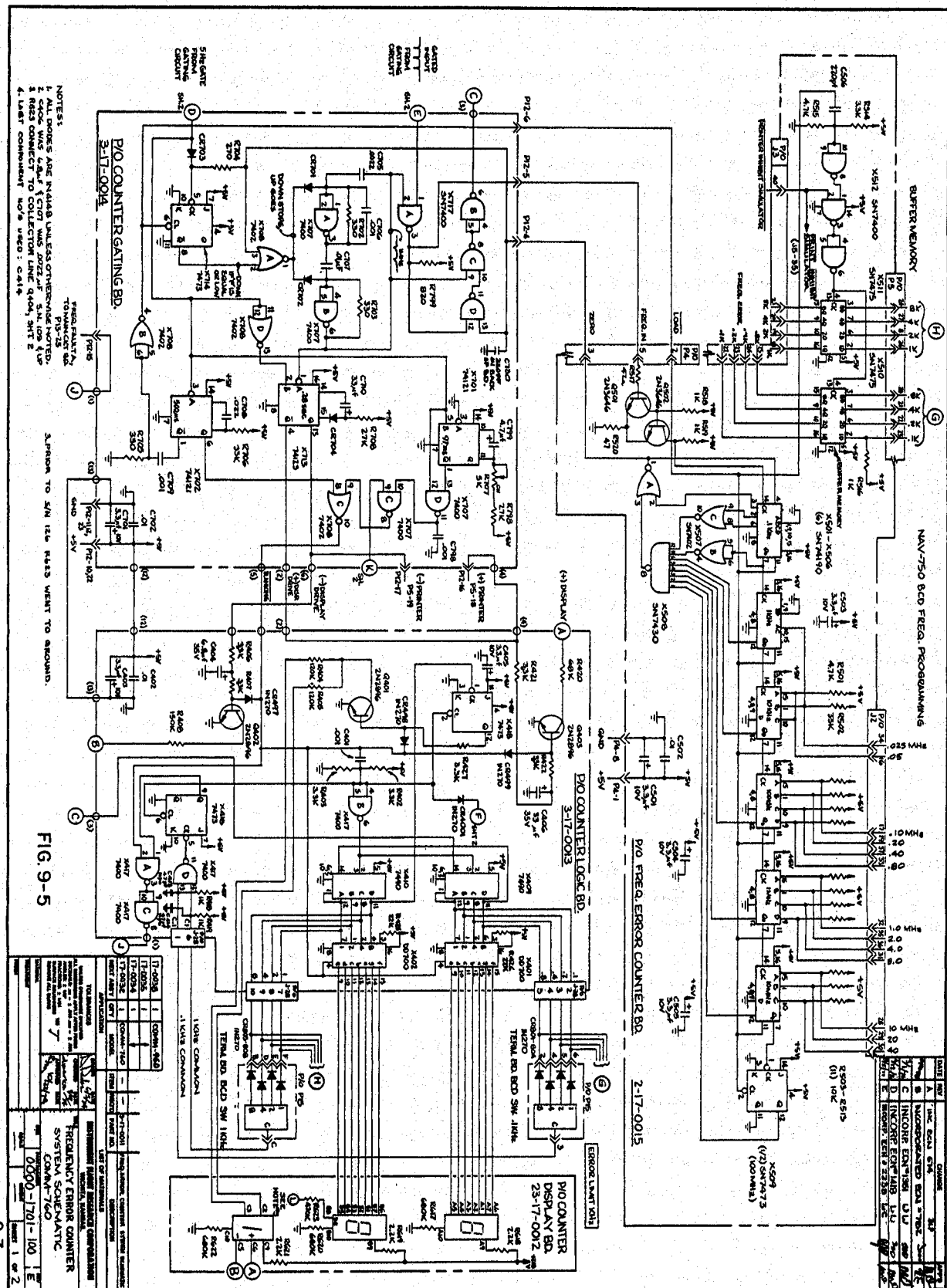
FREQUENCY ERROR COUNTER BOARD





[illegible]

IT-0041	1	COMMA-760	1	1	IT-0041	SCHEMATIC
NEXT ASSY QTY	MODEL	ITEM	REC'D	PART NO.	DESCRIPTION	
LIST OF MATERIALS						
APPLICATION		INSTRUMENT FLIGHT RESEARCH CORPORATION WICHITA, KANSAS				
TOLERANCES		TITLE				
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS APPLY AFTER FINISH		FRONT PANEL				
DIMENSIONS 1/16		TERMINAL BOARD				
FRACTURES 1/16		2-17-041				
CONTACT DIMENSIONS		DATE				
MATERIAL		APPROVED DATE				
TREATMENT		SIZE				
FINISH		PART NUMBER				
		D 7010-17041-100				
		SHEET 1 OF 1				



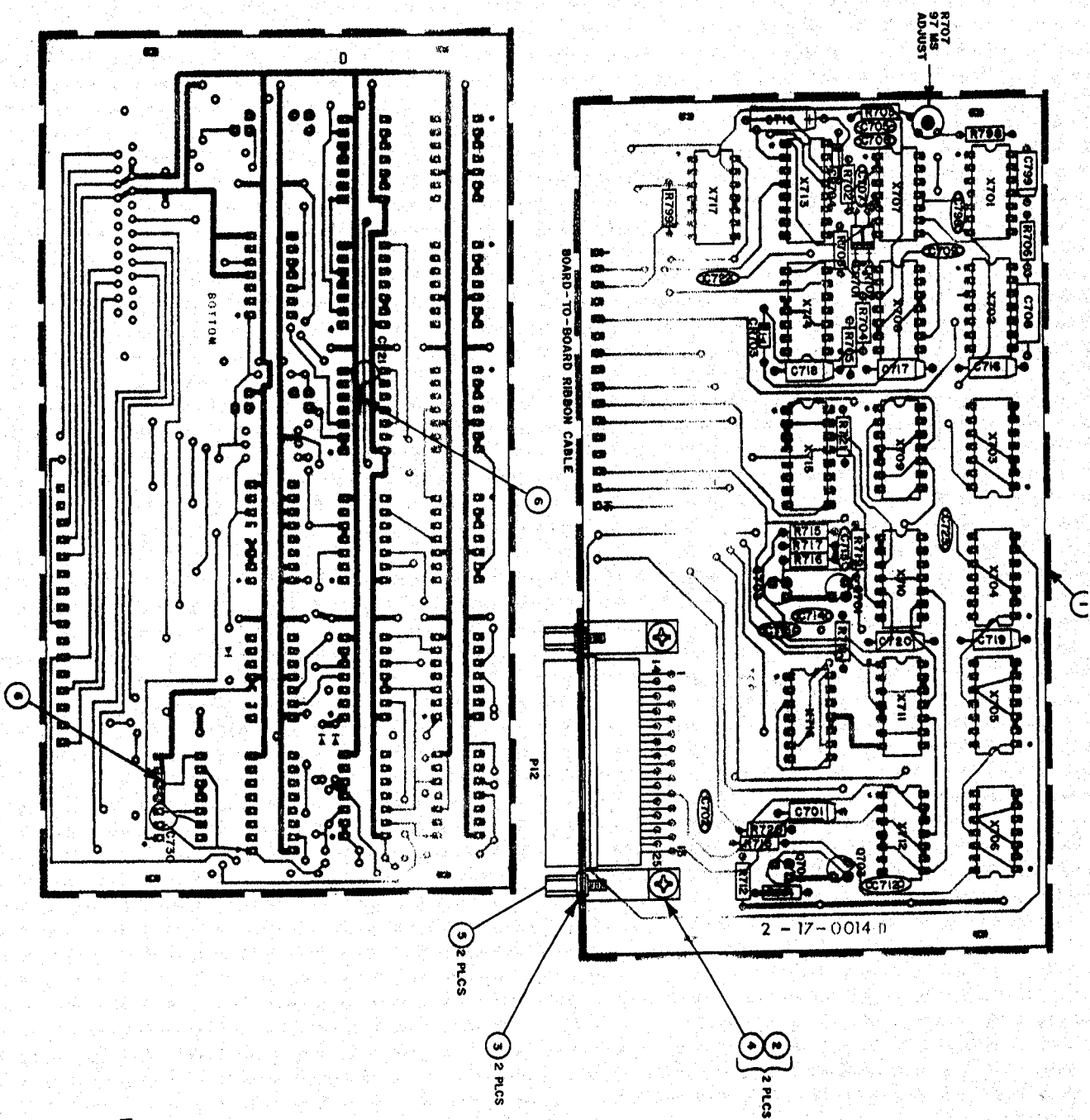


FIG. 9-5.2
COUNTER GATING BOARD
PHYSICAL LAYOUT
(7010-1703-400-D)

Diagram of the back of a circuit board showing component locations. The board is rectangular with various components labeled with callouts. At the top are two circular components labeled 'P4' and 'P5'. Below them are two rows of rectangular components labeled 'X501' through 'X504'. In the center are two vertical rectangular components labeled 'J2' and 'J3'. To the right of these are two more vertical rectangular components labeled 'P1' and 'P2'. At the bottom are two horizontal rectangular components labeled 'J4' and 'J5'. The board also features several circular components labeled 'Q501' through 'Q504' and 'Q505' through 'Q508'. The text 'TOP' is printed in the center of the board.

[illegible]

Q404	X417	X409	X401
Q405	X418	X410	X402
Q406	X419	X411	X403
	X420	X412	X404
	X421	X413	X405
	X422	X414	X406
	X423	X415	X407
	X424	X416	X408

BOARD-TO-BOARD
RIBBON CABLE

NEXT ASSY QTY		COMM-760		MODEL		ITEM REQD		PART NO.		DESCRIPTION	
APPLICATION						LIST OF MATERIALS					
TOLERANCES						INSTRUMENT FLIGHT RESEARCH CORPORATION WICHITA, KANSAS					
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS APPLY AFTER FINISH						TITLE					
MATERIALS: 2 .000						COUNT LOGIC BD.					
FINISHES: 1 / 100 1007						PHYSICAL LAYOUT					
SURFACE RECOMMEND						COMM-760 2-17-035					
MATERIALS						SIZE					
PC. 23-17-0015						PART NUMBER					
TOLERANCE						DATE					
TOLERANCE						REVISION					
TOLERANCE						SHEET 1 OF 1					

0.1 KHz
1.0 KHz
10.0 KHz
0.1 KHz
1 KHz
10 KHz
100 KHz
1 MHz
10 MHz
100 MHz

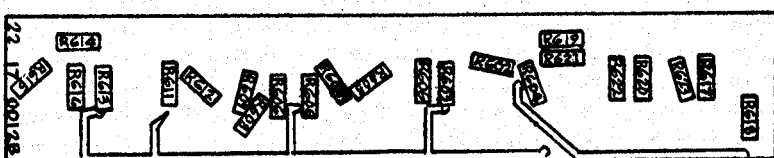
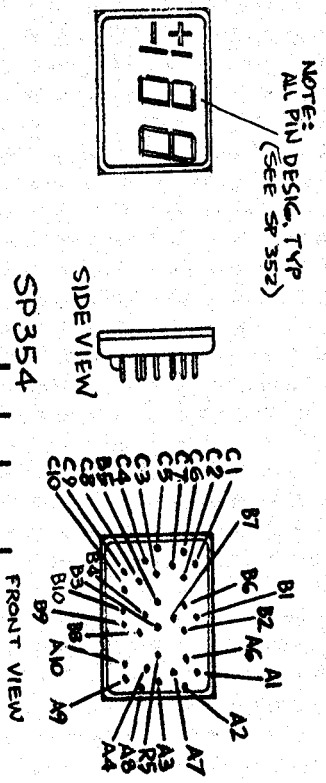
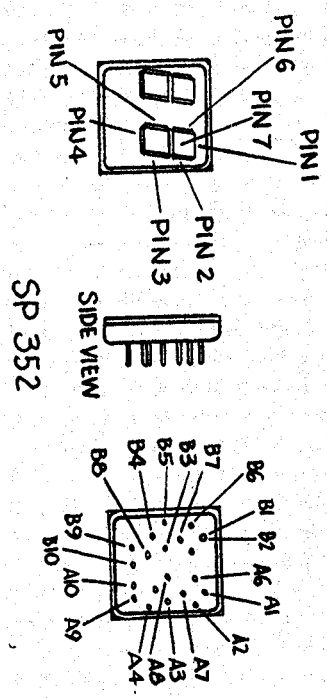
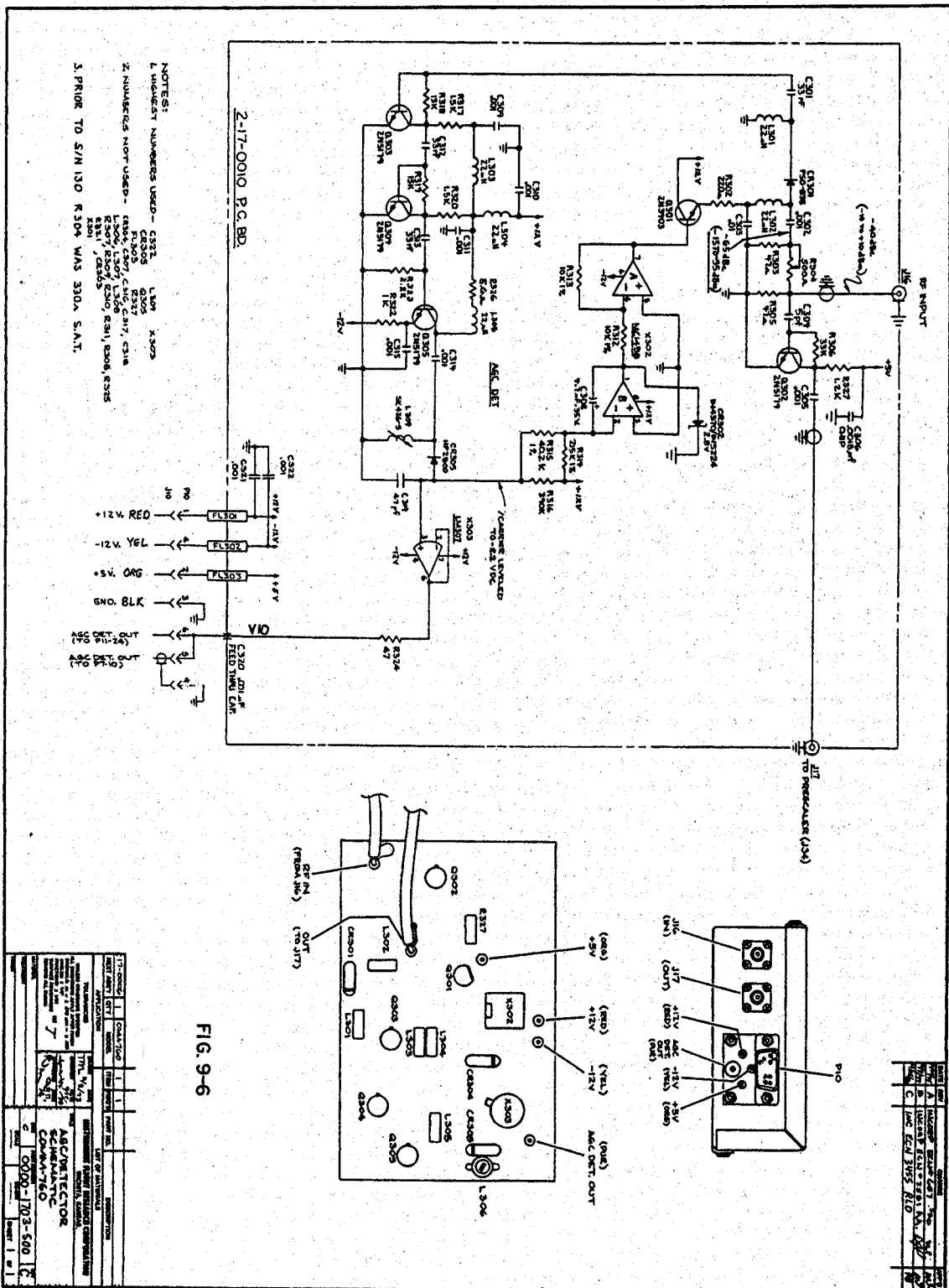


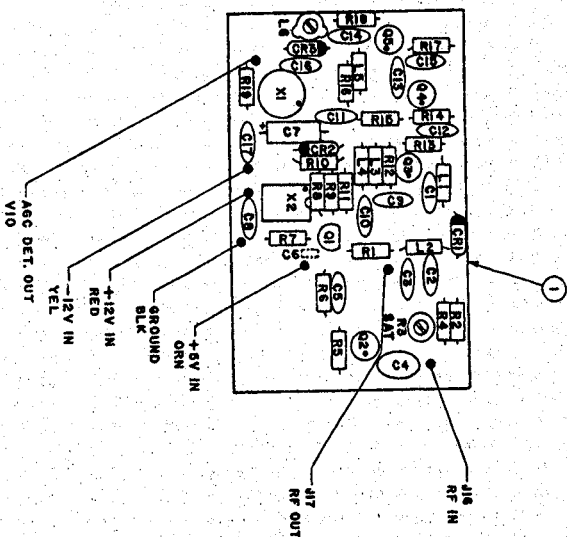
FIG. 9-5.5



NEXT ASSY QTY		MODEL		ITEM REQD		PART NO.		DESCRIPTION	
APPLICATION					LIST OF MATERIALS				
TOLERANCES UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ± .005 ANGLES ± .090 RECESSES ± .005 RECTIFIERS ± .005 SURFACE DIMENSIONS REPAIR ALL WELD MATERIAL					DRAWING NO. <u>5144003</u> DATE CHECKED DATE APPROVED DATE <u>4/8/74</u>				
TITLE					INSTRUMENT FLIGHT RESEARCH CORPORATION WICHITA, KANSAS				
COUNTER DISPLAY BOARD PHYSICAL LAYOUT									
SIZE		FOOTING		DATE		REV			
8 1/2 x 11		2-17-0016							
TOLERANCE		SCALE		SHEET		OF			
.005		1/4" = 1"		1		1			



REV	DATE	DESCRIPTION	BY	CHK
1		UPDATED REV LETTERS		
2		TO ADD E WITH P		
3		INC ECN 9335		
4		REDRAWN		
5		INC NC 9574		

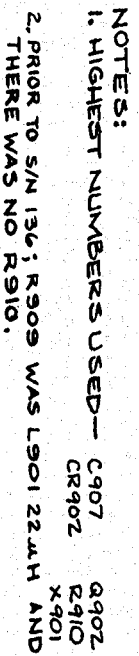


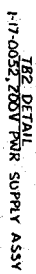
- NOTES:
1. ALL RESISTORS ARE 1/4 W, 10 % TOLERANCE EXCEPT AS NOTED.
 2. ALL CAPACITOR VALUES ARE IN μ F EXCEPT AS NOTED.
 3. SOLDER LEADS MAY EXTEND .04 TO .08 INCHES FROM BOTTOM OF BOARD AFTER SOLDERING.
 4. MAXIMUM HEIGHT OF COMPONENTS TO BE .35 INCHES FROM COMPONENT SIDE OF BOARD.
 5. PLACE CHIP CAPACITORS ON BACK SIDE OF BOARD.
 6. REF SCHEMATIC 0000-1700-500.

FIG. 9-6.1

ASG DETECTOR BD ASSY	
REV	1
DATE	10/10/00
BY	10/10/00
CHK	10/10/00
APP	10/10/00
REV	1
DATE	10/10/00
BY	10/10/00
CHK	10/10/00
APP	10/10/00

The schematic diagram illustrates the output stage of a 100-Watt Class AB1 push-pull amplifier. The circuit is powered by a +5V supply and a -35V supply. The output is taken from the JFETs and passes through a network of resistors (R901-R909) and capacitors (C901-C907) to a 15V output. The circuit is powered by a +5V supply and a -35V supply. The output is taken from the JFETs and passes through a network of resistors (R901-R909) and capacitors (C901-C907) to a 15V output.

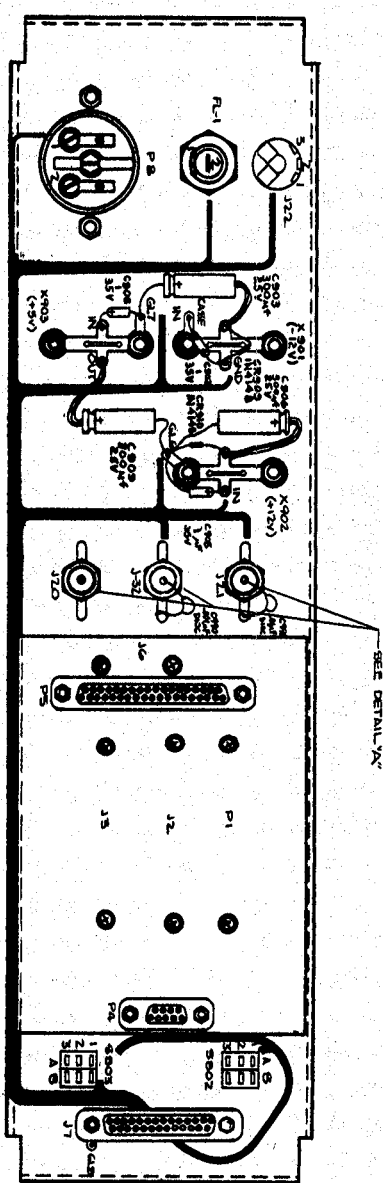
[illegible]



NOTES:
1. PLACE WIRE BUNDLES AS SHOWN.
REFER TO P-17-0035 WIRING LIST FOR
SPECIFIC GAUGE, COLOR, AND LENGTH
REQUIRED.
2. CUT OFF T902-3 CLOSE TO TRANS FORMER BODY.
THIS LEAD NOT USED.

9-17

REV	DATE	DESCRIPTION
1	1-1-62	SEE DETAIL 1-1-62
2	1-1-62	SEE DETAIL 1-1-62
3	1-1-62	SEE DETAIL 1-1-62
4	1-1-62	SEE DETAIL 1-1-62
5	1-1-62	SEE DETAIL 1-1-62
6	1-1-62	SEE DETAIL 1-1-62
7	1-1-62	SEE DETAIL 1-1-62
8	1-1-62	SEE DETAIL 1-1-62
9	1-1-62	SEE DETAIL 1-1-62
10	1-1-62	SEE DETAIL 1-1-62



BEND GROUND LUG UP AND SECURE TO COAX WITH 17-0005. SOLDER LEAD TO CENTER CONDUCTOR AND SHIELD TO GROUND LUG.

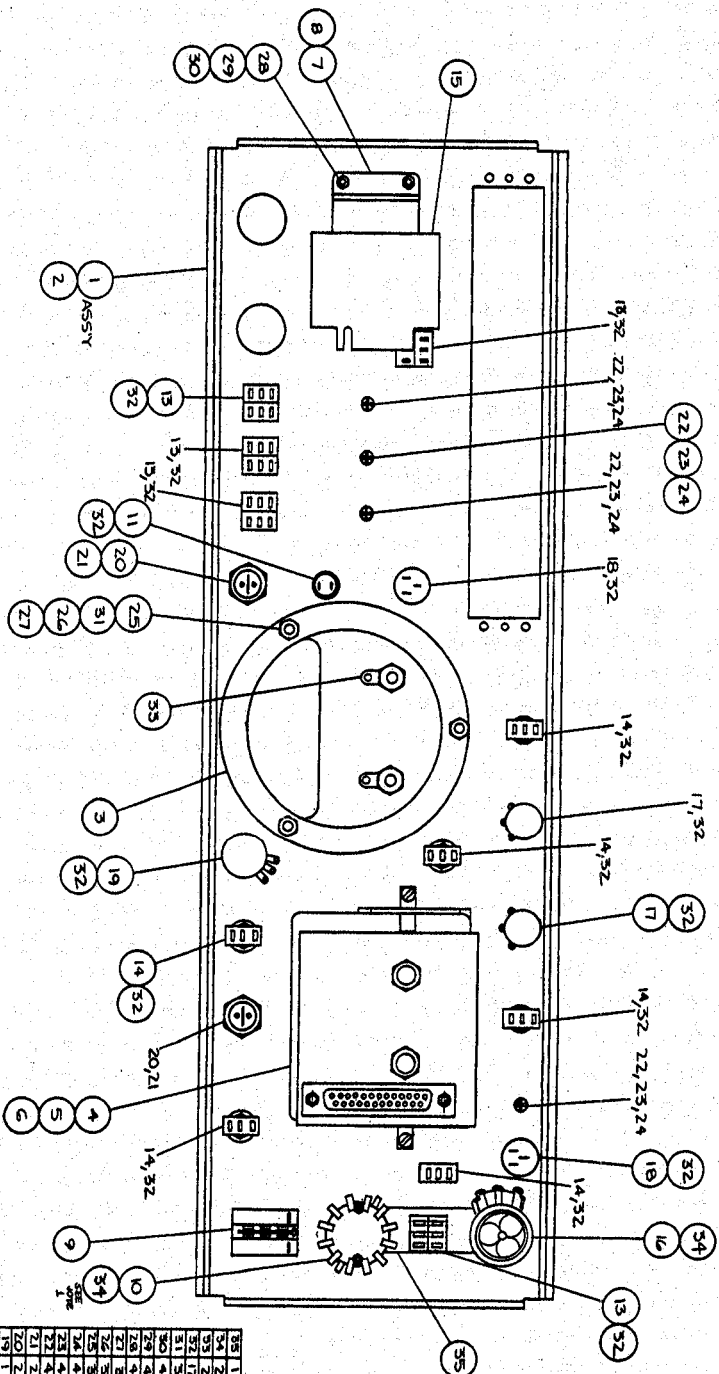
DETAIL "A"

NOTE:
PLACE BANDLES IN APPROX. POSITION SHOWN. REFER TO 17-0005 WIRING LIST FOR SPECIFIC COLOR, LENGTH, AND SIZE NECESSARY.

FIG. 9-12

REV	DATE	DESCRIPTION
1	1-1-62	SEE DETAIL 1-1-62
2	1-1-62	SEE DETAIL 1-1-62
3	1-1-62	SEE DETAIL 1-1-62
4	1-1-62	SEE DETAIL 1-1-62
5	1-1-62	SEE DETAIL 1-1-62
6	1-1-62	SEE DETAIL 1-1-62
7	1-1-62	SEE DETAIL 1-1-62
8	1-1-62	SEE DETAIL 1-1-62
9	1-1-62	SEE DETAIL 1-1-62
10	1-1-62	SEE DETAIL 1-1-62

REV	DATE	BY	CHKD	DESCRIPTION
1				INITIAL REV
2				REVISIONS
3				REVISIONS
4				REVISIONS
5				REVISIONS
6				REVISIONS
7				REVISIONS
8				REVISIONS
9				REVISIONS
10				REVISIONS
11				REVISIONS
12				REVISIONS
13				REVISIONS
14				REVISIONS
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96				REVISIONS
97				REVISIONS
98				REVISIONS
99				REVISIONS
100				REVISIONS



NOTES:
1. SET STOPS PER PAGE (A) POSITIONS.

FIG. 10-1

REV	DATE	BY	CHKD	DESCRIPTION
1				INITIAL REV
2				REVISIONS
3				REVISIONS
4				REVISIONS
5				REVISIONS
6				REVISIONS
7				REVISIONS
8				REVISIONS
9				REVISIONS
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97				REVISIONS
98				REVISIONS
99				REVISIONS
100				REVISIONS

DATE	REV	CHANGE	BY	CHK
10-10-70	1	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	2	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	3	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	4	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	5	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	6	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	7	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	8	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	9	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	10	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	11	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	12	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	13	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	14	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	15	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	16	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	17	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	18	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	19	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	20	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	21	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	22	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	23	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	24	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	25	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	26	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	27	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	28	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	29	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	30	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	31	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	32	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	33	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	34	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	35	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	36	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	37	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	38	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	39	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	40	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	41	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	42	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	43	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	44	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	45	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	46	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	47	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	48	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	49	REWORKED FOR 1 JAN 71	WJ	WJ
10-10-70	50	REWORKED FOR 1 JAN 71	WJ	WJ

NOTE:
 1. PLACE A LOCKWASHER BETWEEN THE SCREW HEAD AND BRACKET, AND BETWEEN THE BRACKET AND SPAL.

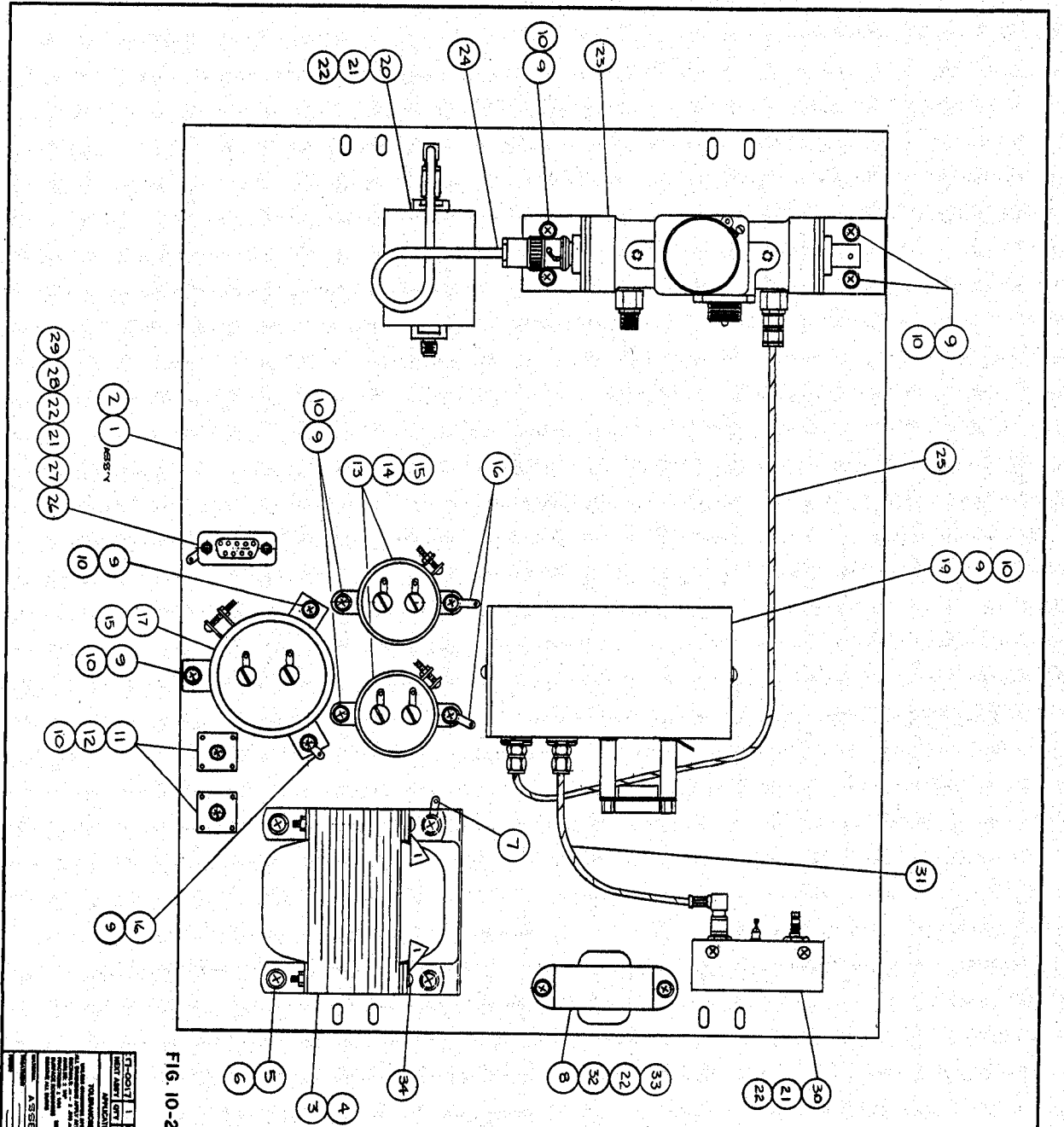


FIG. 10-2

ITEM	QTY	DESCRIPTION	UNIT	REMARKS
1	1	SCREW		
2	1	WASHER		
3	1	BRACKET		
4	1	SCREW		
5	1	WASHER		
6	1	BRACKET		
7	1	SCREW		
8	1	WASHER		
9	1	BRACKET		
10	1	SCREW		
11	1	WASHER		
12	1	BRACKET		
13	1	SCREW		
14	1	WASHER		
15	1	BRACKET		
16	1	SCREW		
17	1	WASHER		
18	1	BRACKET		
19	1	SCREW		
20	1	WASHER		
21	1	BRACKET		
22	1	SCREW		
23	1	WASHER		
24	1	BRACKET		
25	1	SCREW		
26	1	WASHER		
27	1	BRACKET		
28	1	SCREW		
29	1	WASHER		
30	1	BRACKET		
31	1	SCREW		
32	1	WASHER		
33	1	BRACKET		
34	1	SCREW		

NOTE:
1. USE MOD-1/4 FOR 220V
OPERATION.

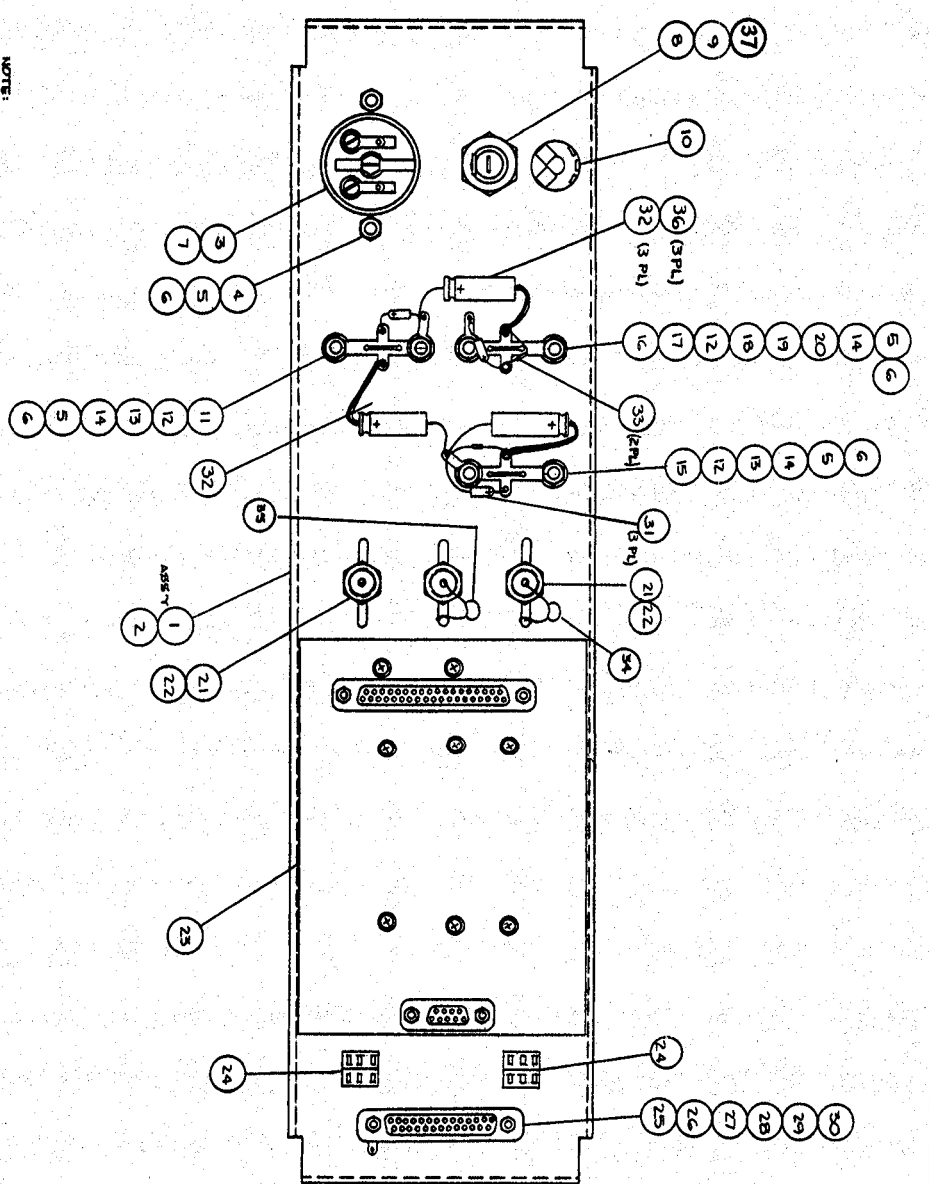


FIG. 10-3

SEE NOTE 1

ITEM NO.	DESCRIPTION	QTY	UNIT	ASSEMBLY
10	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
11	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
12	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
13	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
14	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
15	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
16	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
17	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
18	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
19	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
20	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
21	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
22	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
23	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
24	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
25	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
26	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
27	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
28	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
29	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
30	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
31	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
32	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
33	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
34	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
35	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
36	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3
37	1-1/2" DIA. 1/4" THICK PLATE	1	PLATE	10-3